

CHAMP DSP - FPGA - SDR PRODUCTS PAGE 2007. **VPX REDI**



CHAMP-FX/V4 FPGA accelerator VXS:
 Vita 41 VXS/VME card.
 Two Virtex-4 FX FPGAs (V4FX100).
 Two IBM 405 PowerPCs per FPGA.
 Two PMC/XMC sites.
 FPGA design kit, VHDL Libraries.
 Air or Conduction Cooled.

The CHAMP-FX/V4 provides an FPGA processing platform with a balanced mix of mezzanine interfaces, high bandwidth I/O and a variety of DDR FPGA memories, off board fabric connectivity and FPGA processing resource. Thermal management of the FPGA, including power consumption monitoring to enable use of FPGA in Rugged environments where total control of hardware is required. FPGAs are easily reconfigurable and a VHDL design kit enables rapid prototyping of FPGA base system.



CHAMP-AV6 Quad/ Octal PowerPC 8641 VPX:
 Vita 46 VPX card.
 Four PowerPC 8641/8641D CPUs with upto 8 cores.
 Four Serial RapidIO ports to the VITA 46 core fabric.
 Option of PCIexpress to the core fabric.
 GbE per CPU, Onboard GbE switch, Four EIA-232.
 Air or Conduction Cooled.

The CHAMP-AV6 quad Power PC board combines the latest in Altivec-enabled processors with serial switched fabric in the VITA 41 VPX format. Multi-processor systems based on this card can utilise 10GB/s full duplex bandwidth via four serial RapidIO or PCIexpress ports. These are utilised for card to card communications while on board there is a switched fabric based on a Tundra TS1578-8 port SRIO switch. Multiple CHAMP-AV6 cards may be inter-connected using the SRIO core fabric interface. A bandwidth of 5 GB/s transmit and receive (total 10GB/s) can be achieved.



CHAMP-FX VirtexII VXS:
 Vita 41 VXS/VME 64x
 Two Xilinx Virtex-II Pro Platform FPGAs
 Two PMC/XMC mezzanine sites with Processor PMC compatibility
 Two IBM 405 PowerPCs per FPGA.
 Four 4-bit, bi-directional RocketIO ports.
 FPGA design kit, VHDL Libraries.
 Air or Conduction Cooled.

The CHAMP-FX is supported with the CHAMPTools-FX design kit which includes reference designs and ready-to-use VHDL modules to implement memory interfaces, DMA, PCI, RocketIO and support for the Xilinx II Pro's two internal IBM PowerPC 405 processors. The kit removes much of the risk associated with FPGA design, with modules that are designed and qualified for operation at temperature extremes where typical off the shelf IP can fail to meet timing requirements.



CHAMP-AV-IV VME64x:
 VME 64x interface.
 Quad PowerPC™ 7447A/7448 processors at up to 1.25 GHz
 QuadFlow architecture with 3.2 GB/s peak on-board throughput
 Each processor has Gbe connection to on-board GbE switch
 Two ports from GbE switch routed to backplane
 Two 64-bit, 100 MHz PCI-X mezzanine modules (PMC-X)
 Air or Conduction Cooled.

The CHAMP-AV IV is the third generation of quad PowerPC DSP board with the QuadFlow architecture providing high bandwidth connections between four 7447A/7448 processors. Each processor, capable of up to 10 GFLOPs peak, is equipped with its own bank of DDR SDRAM with 2GB/sec peak bandwidth. Processors are interconnected via 100MHz PCI-X busses. Utilizing the QuadFlow ability to handle up to four simultaneous transfers, the AV IV can deliver up to 3.2GB/sec of on-card inter-processor bandwidth.



CHAMP-TOOLS VxWorks:
 Software Development for the CHAMP family.
 VxWorks Board Support Package.
 Supports GNU compiler.
 Performance Monitoring Functions.
 Board Support Library.
 FLASH management Utility.

The VxWorks BSP supports VxWorks 5.4/5.5 and the Tornado 2.02/2.2 Integrated Development Environment with the GNU compiler. Users have the option of using VxWorks on any number of PowerPC processors. The BSP provides a full set of function calls for interfacing with the CHAMP hardware features, including Ethernet, Serial I/O, DMA controllers, VME and cPCI. The VxWorks BSP has the capability to capture and report critical timing elements which are important to real time DSP processing. Special attention has been paid to providing DMA services as data movement is invariably a critical component of managing a real time processing problem.



CHAMP-ELDK Linux Software Suite:
 Linux Operating System for the CHAMP-AV-IV
 Linux Kernel 2.6.x, contains DENX, ELDK 4.0.
 GNU gcc4.0, gfb command line debugger.
 CHAMP specific drivers.
 Reference Embedded FLASH file system.
 Curtisswrite inhouse Linux Development team.

The Linux kernel and board specific device drivers offer a Linux applications Engineer a complete development environment for the creation of embedded Linux applications for high performance multi processor applications. The Embedded Linux Developers Kit is based upon the DENX solution for PPC, with a suite of hardware device drivers for the CHAMP-AV-IV developed and supported by Curtisswrite. The ELDK supports a cross hosted dev environment to x86 PC.



CHAMP-IPC Library:
 Interprocessor Communications Middleware.
 Low latency message passing library.
 POSIX style application interface.
 Priorities, Time-outs, copyless transfers.
 Bulk Data Transfer.
 Memory less signalling from any processor to any other processor.
 Segmented block transfer capability.

Real-time sensor based systems require status, control and bulk data movement to coexist within the same communications architecture. The IPC library provides all the capabilities needed to control applications running on multiple processors having data movement requirements. The software hides the hardware architectural details from the application designer. This hardware abstraction provided by IPC ensures programs written on current hardware will be forward compatible on next generation CHAMP hardware.



CHAMP-TOOLS FX:
 CHAMP-FX FPGA Design Kit and Support SW.
 Simulation testbench with scriptable simulation.
 Software library of board support and utility functions.
 Highly optimised Interface and Controller cores including, DDR SRAM, SDRAM, PCI, RocketIO, DMA, SW interconnect.
 Auto-Generated ChipScope modules for internal busses.
 FPGA configuration file loader.
 FLASH file management, memory mapping and data flow.

The FPGA design kit provides the FPGA designer and systems developer with a rich assortment of IP modules and software tools that can accelerate the complex task of developing FPGA-based applications and integrating them into a larger heterogeneous architecture. The CHAMP-FX architecture is suited to DSP applications that place high premium on sustained I/O throughput, FPGA memory bandwidth and off-board fabric connectivity. The CHAMP-FX TOOLS provides a rich library of VHDL IP modules focused specifically on interface controllers and communications infrastructure



TEK Microsystems Inc: Designs, manufactures and markets a wide range of advanced high-performance I/O products for embedded real-time computing systems. The comprehensive product line includes advanced carrier, payload and switch boards based on widely adopted industry standards, more than 30 PMC/XMC cards, advanced ADC/DAC interfaces, and complete data acquisition and data recording/storage systems as well as advanced signal processing systems.

Triton



Tekmicro 2GHz Rx/Tx SDR VXS card.
 Single Channel, 2 GS/s ADC/DAC and Xilinx Virtex-II Pro FPGA Processing Engine
 1x 10 bit 2 GS/s Atmel ADC/DMUX
 1x 12 bit 2 GS/s Euvis MUX/DAC
 VME/VXS form factor, VITA 41.0
 8x 3.125 Gbit/s serial I/O links
 2x Front Panel SFP slots for 2.5 Gbit/s fiber or copper transceivers
 2x DDR SDRAM SODIMM up to 2 GB each
 2x On-Board DDR SDRAM Banks, 0.5 GB.

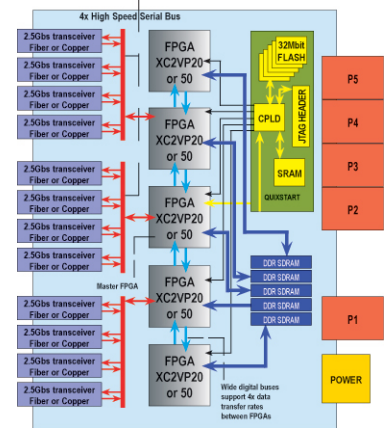
Neptune



Tekmicro 2GHz Rx SDR VXS card.
 Dual Channel, 2 GSPS Digitizer and Xilinx Virtex-II Pro FPGA Processing Engine
 2x 10 bit 2 GSPS Atmel ADC/DMUX
 Xilinx XC2VP70 FPGA
 VME/VXS form factor, VITA 41.0
 8x 3.125 Gbit/s serial I/O links
 2x Front Panel SFP slots for 2.5 Gbit/s fiber or copper transceivers
 2x DDR SDRAM SODIMM up to 1 GB each
 2x On-Board DDR SDRAM Banks, 0.5 GB.

Tekmicro Collisto VXS Switched Fabric Card.

CALLISTO VXS-1 is designed to provide a platform which can be used to concentrate the high bandwidth data generated by multiple VXS payload cards in a VXS based hardware architecture. In addition, CALLISTO VXS-1 allows break out of high bandwidth data to processing sub-systems in separate chassis through fiber optic or copper transceiver modules on the front panel. Five Xilinx Virtex-II Pro FPGAs are used to provide the high bandwidth communications links on the CALLISTO VXS-1 and the FPGAs are also available to provide a significant data processing resource. The CALLISTO VXS-1 is supplied with a set of basic FPGA bitstreams, which can be used to verify correct operation of all hardware components and data links on the card. A hardware reference manual is supplied with the card that provides all of the information and references necessary for users to begin developing their own FPGA design for the card. To accelerate the development process, a Developer's Kit can be purchased for the CALLISTO VXS-1 which provides FPGA cores, software and source code reference design examples. This allows rapid interfacing of user applications to the on-board memory resources and off-board data links. The kit includes a design example showing how to achieve simple raw mode data links via the backplane to other FPGA based VXS payload cards, such as those in the Quixilica range. A further example illustrates use of the front panel data links to link the card to an external host via a UDP/Gigabit Ethernet link.

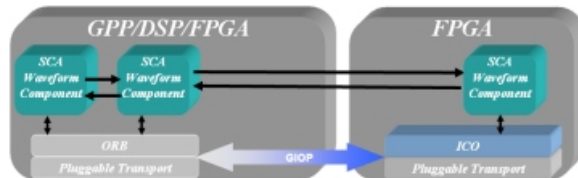


JazzFiber



The JazzFiber Quad Serial FPDP PMC module: The PMC combines the advantages of the ANSI/VITA 17.1 Serial FPDP interconnect with highly integrated FPGA technology to provide channel density and throughput at data rates up to 247 MB/s in a single PMC module.

“Very Interesting Product”, ORB (Corba Light) FPGA core



ICO Integrated Circuit Orb: The ICO supports a drop-in Software Communications Architecture (SCA) compatible interface between distributed software objects running on processors and waveform objects residing in FPGA. The connection between Software client and Hardware servant will now be seamless, fast and use fewer system resources. ICO further eliminates the need to embed general purpose processing cores into FPGAs in order to offer software ORB capability. Although a viable approach, this approach tends to require significant gate count and memory utilization and generally these processing cores cannot be clocked fast enough to deal with the ever-increasing performance requirements of SDR applications. The embedded ORB has been written in portable VHDL that can be synthesized onto any FPGA or ASIC platform.

PowerMatrix 24/48 DSP System: The PowerMatrix-24 and PowerMatrix-48 SMP are two of the offerings in the PowerMatrix family of fully integrated open-architecture systems. The PowerMatrix-24 and 48 provide developers with an application-software ready multi-processor system with easily customizable I/O. Based on twelve dual or quad SMP PowerPC boards, the PowerMatrix-24 and 48 are ideally suited for applications that require a high level of CPU processing and sharing of data between the processing units. With twelve and twenty-four open PMC sites respectively, the PowerMatrix-24/48 system can be configured with many standard I/O options including Serial FPDP, Fibre Channel, MIL-STD-1553 and high-speed A/D channels. These user definable options, combined with the standard Gigabit Ethernet, Serial I/O and (SATA or FireWire), allow the PowerMatrix-24 and PowerMatrix-48 to receive raw data and transmit results to other parts of the system in fast and flexible ways.



For more information on these products please contact Unitronix:

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