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# Industrial CompactFlash Card

## AC73-XXXXR04XX



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## 1. Product Description

### 1.1 Product Overview

AC73 series is CompactFlash Storage Card based on FLASH memory controller technology. This card complies with CompactFlash specification. It is suitable for the usage of data storage memory for PC or other electric equipment and Digital Still Camera (DSC). This card is equipped with NAND FLASH memory. By using this card it is possible to operate stability for the system that has CompactFlash slots.

AC73 series support Fixed and Removable mode, Fixed mode disk use in system storage, some operating system can not accept boot-up from Removable mode disk like Windows XP, when we boot-up from CompactFlash Storage Card with Windows XP, the system detect the device will disable Removable device boot-up function, so the system can not finish the boot-up process. For this issue, we can setting the device mode to Fixed mode to solve this problem. The CFC setting to Fixed or Removable mode will no any function different or issue.

#### ● **Application Fields;**

- Industrial PC and Thin Client
- Entertainment/Consumer Electronic Device
- Game and Telecommunication Machine
- Ticketing, Examining, testing machine
- Army, Health and Production Equipment and Machine
- Other machines and Equipments with CompactFlash™ Card Interface

### 1.2 Product Feature

- 128MB~8GB flash memory card
- High performance.
- High reliability.
- Noiseless.
- Robust Error Correction.
- Low power consumption.
- Voltage 3.3V or 5.0V operation.
- PC Card ATA protocol compatible.
- True IDE mode compatible.
- Following type I CompactFlash™ storage card dimensions.
- CompactFlash™ specification 3.0 version compliant.
- Support PIO Mode 4, Multi-Word DMA 2, and Ultra DMA 2
- Hardware write protect function.
- High Read/Write Speed
- Noiseless operation

**Notice** : The performance will depend on different platform with different test result.

### 1.3 System Requirement

- The Host system which is connected to Industrial CompactFlash™ Storage Card should meet system requirements at minimum;

#### 1.3.1 Power Requirement

- Voltage: DC +3.3V ± 5% or DC +5.0V ± 10%

#### 1.3.2 Operating System

- Windows 98SE/ME/2000/XP/Vista
- Linux, DOS
- WinXP Embedded/WinCE

#### 1.3.3 Interface

- CFA3.0 compatible 50pin SMT connector and type I (3.3mm).

## 2. Specification

### 2.1 Physical Specification

#### 2.1.1 Overlook

The overlook views of High Speed Industrial CompactFlash™ Storage Card are illustrated in Figure 1.

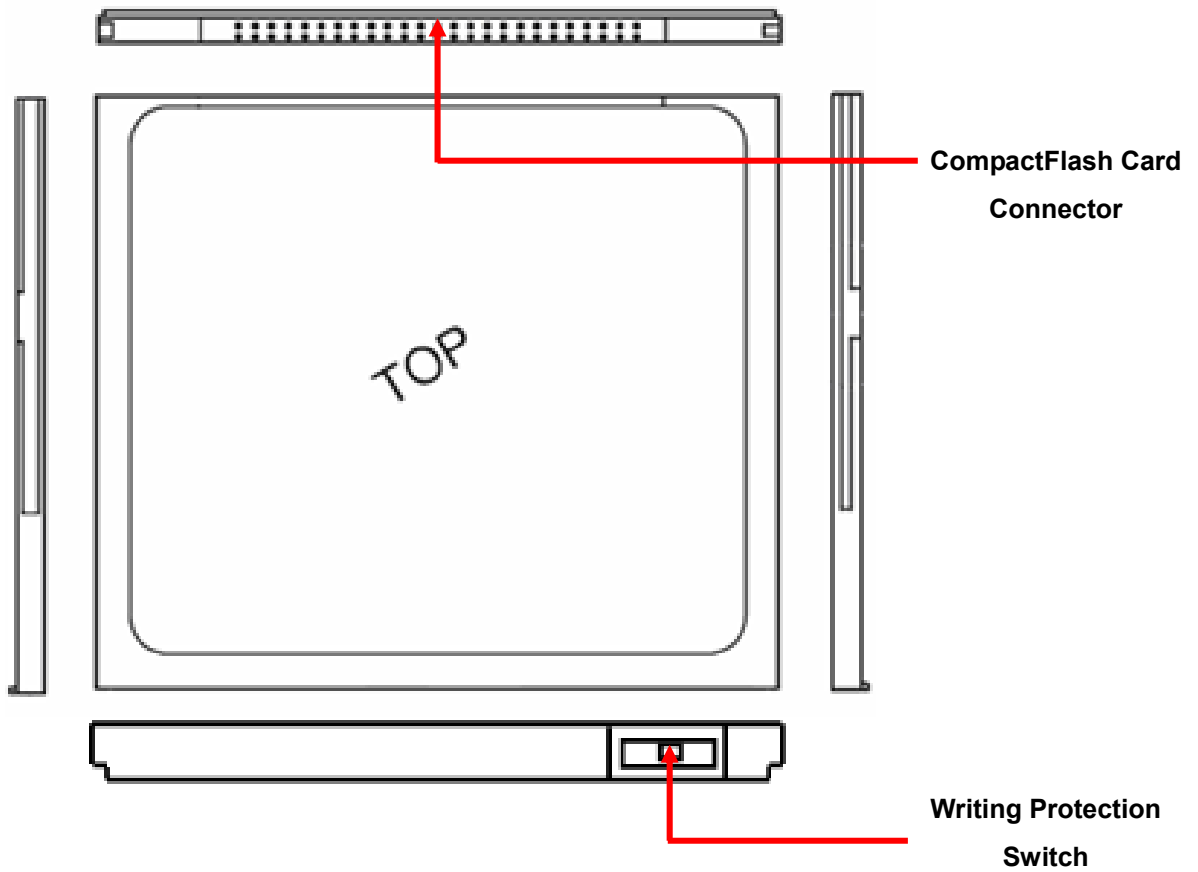


Figure 1: CompactFlash™ Storage Card Overlook Diagram

2.1.2 Dimension

The Dimensions of CompactFlash™ Storage Card are illustrated in Figure 2 and described in Table 1.

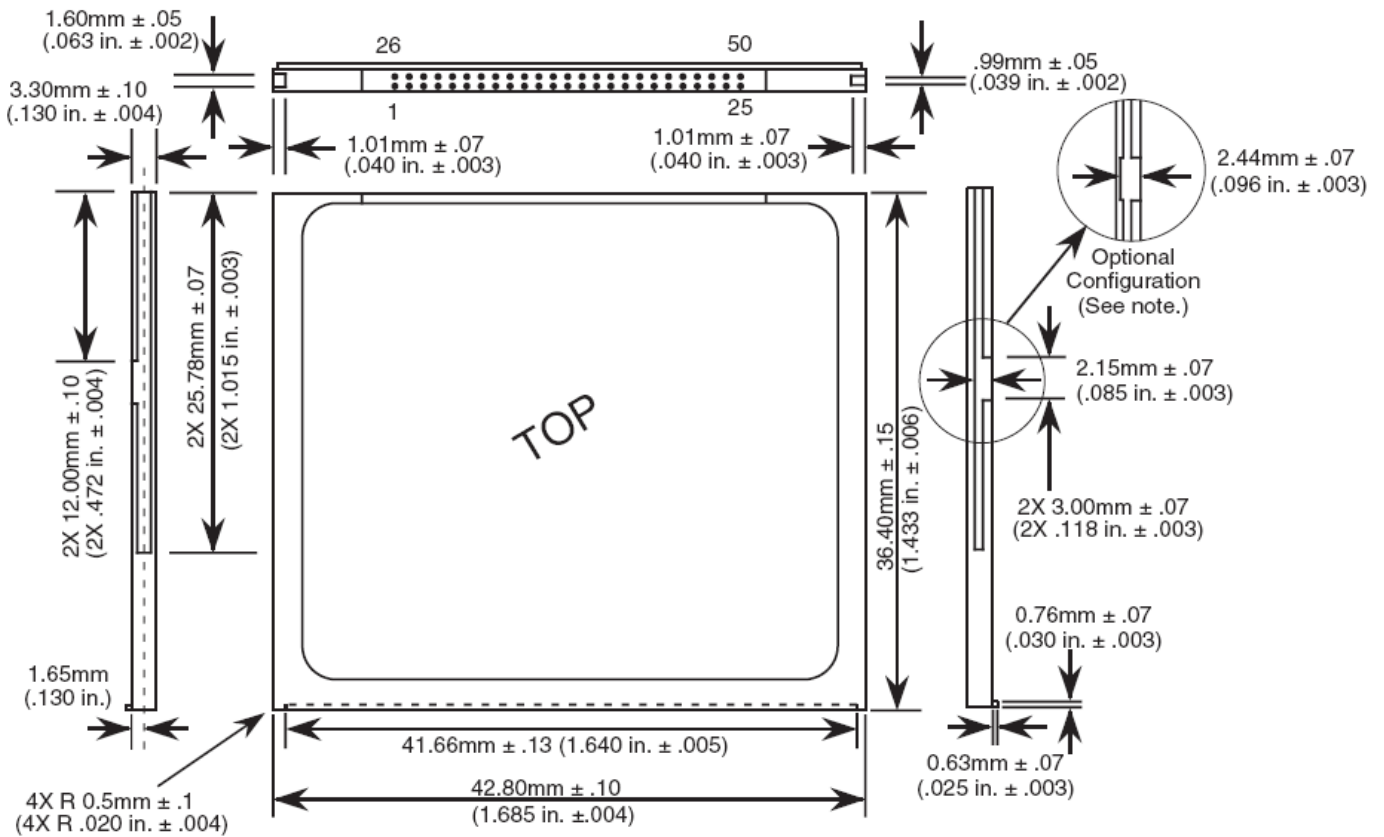


Figure 2: CompactFlash™ Storage Card Dimensions

**Notice** : The optional notched configuration was shown in the CFA specification Rev. 1.0 in specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but is not recommended.

Table 1: CompactFlash™ Storage Card Physical Dimension

<b>Length</b>	36.4 ±0.15 mm (1.433 ±0.006in.)
<b>Width</b>	42.8 ±0.10 mm (1.685 ±0.004in.)
<b>Thickness (Including Label Area)</b>	3.3 ±0.10mm (0.13 ±0.004in)

2.1.3 Weight

- Weight: 10.5g

2.2 Electronic Specifications

2.2.1 Product Definition

The CompactFlash™ Storage Card contains a single chip controller and flash memory module(s) in a matchbook-size package with a 50-pin connector consisting of two rows of 25 female contacts each on 50 mil (1.27mm) centers. The controller interfaces with a host system allowing data to be written to and read from the flash memory modules(s).

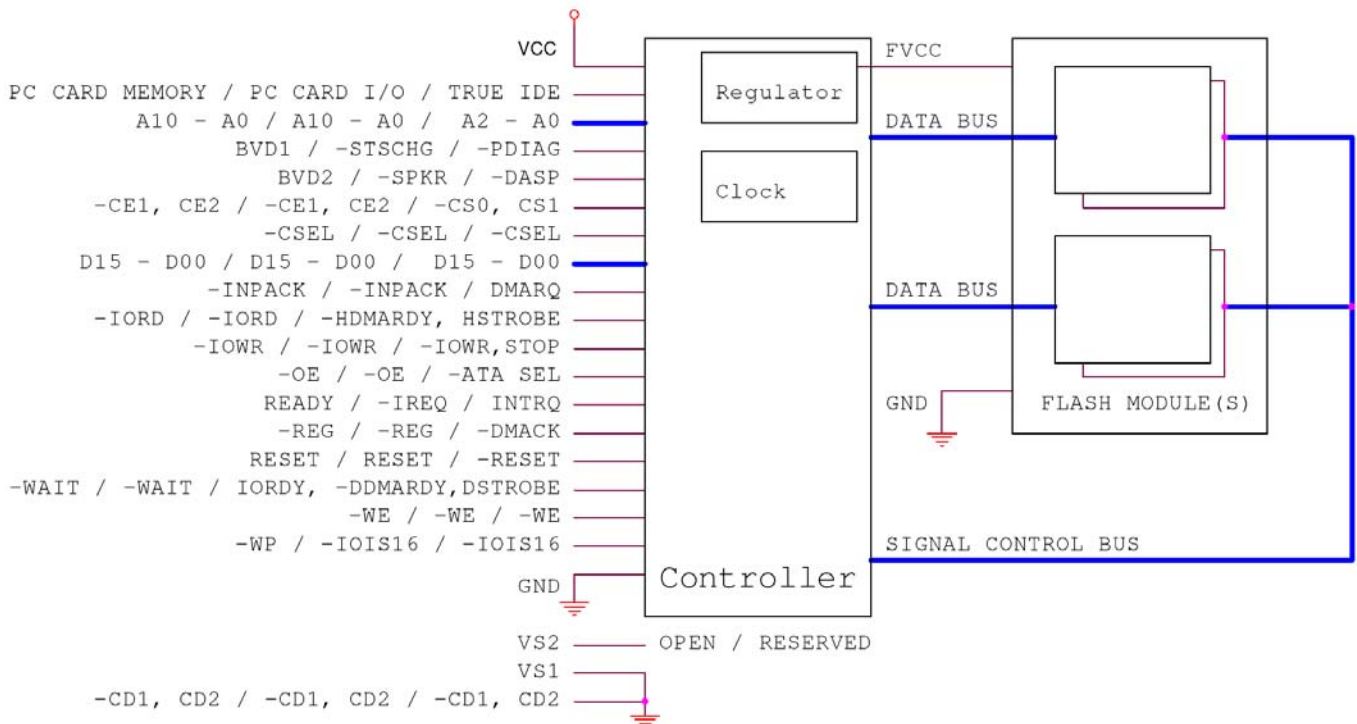
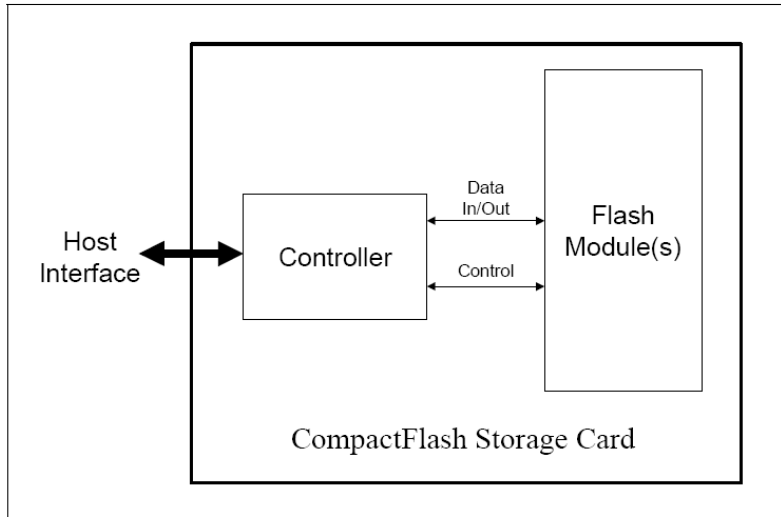


Figure 3: CompactFlash™ Storage Card Block Diagram

## 2.2.2 Operating Voltage

- Voltage DC +3.3V ± 5% or DC +5.0V ± 10%

## 2.2.3 Capacity and Block Size information

- Capacity: 128MB ~ 8GB
- Sector Size: 512B

## 2.2.4 Power Consumption (3.3V/5.0V)

- Current Information

Test Item	3.3V	5.0V
Write Current	45mA	48mA
Read Current	43mA	45mA
Sleep Current	0.4mA	0.6mA

## 2.3 Performance Specifications

### 2.3.1 Modes

- Memory Card Mode
- I/O Card Mode
- True-IDE Mode (PIO Mode: 4, Multi-Word DMA Mode: 2, Ultra DMA Mode: 2)

### 2.3.2 Data Transfer Time

#### Dual Mode

- Sequential Read: Up to 20 MB/sec
- Sequential Write: Up to 10 MB/sec

#### Single Mode

- Sequential Read: Up to 10 MB/sec
- Sequential Write: Up to 5 MB/sec

- Ultra DMA2: 33 MB/sec burst

#### ※ Test Platform:

MB 1: DFI CF4 / Chipset nForce SLI-DR / CPU: AMD146 2.0GHz DDR400: 256MB

MB 2: GIGA 8I945GME / Chipset: Intel 945+ICH7 / CPU: P4-3.0GHz DDR400: 256MB

Testing Software: HD Bench 3.4 / SiSoftware Sandra / Qbench

Testing Operating System: DOS, WinXP

**Notice** The value is various bases on the testing platform.

### 2.3.3 Data Retention

- 10years without requiring power support

### 2.3.4 Wear-leveling

- Dynamic Wear-Leveling for same level of Write/Erase Cycle

### 2.3.5 Bad Block Management

- The Bad Blocks of Flash Memory will be replaced into new ones by controller.

## 2.4 Environmental Specification

### 2.4.1 Temperature

- Operating Temperature: 0°C to +70°C, Non Operating Temperature: -40°C to +85°C (Industrial type)
- Operating Temperature: -40°C to +85°C, Non Operating Temperature: -55°C to +95°C (Wide Temperature type)

### 2.4.2 Humidity

- Operating Humidity (30°C Max. Wet Bulb Temp): 5% to 95%
- Non-Operating Humidity (30°C Max. Wet Bulb Temp): 5% to 95% (with no condensation relative humidity)

2.4.3 Bare Drop Testing

- Testing Conditions: 100cm height
- Testing Orientation: (Free fell) Front/Rear/Right/Left/Top/Bottom side
- Testing Result: Pass

2.4.4 Vibration

- Random Vibration (Operation) : Testing Specification

Frequency (Hz)	PSD (G <sup>2</sup> /Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.01	6Grms	30min per axis (X · Y · Z)
100	0.08		
500	0.08		

- Random Vibration (Non-Operating): Testing Specification

Frequency (Hz)	PSD (G <sup>2</sup> /Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.1	6Grms	30min per axis (X · Y · Z)
100	0.04		
500	0.04		
2000	0.004		

- Frequency Range: 3 ~ 2000Hz
- Testing Result: Pass

2.4.5 Inserted Durability Test

- Testing Condition: 3sec/cycle – Repeated Plug/Unplug 10,000 cycles
- Testing Result: Pass

2.5 Reliability Specification

2.5.1 ECC/EDC (Error Correction Code/Error Detection Code)

- Built-in Reed Solomon 4bytes/sector correction and 5bytes/sector detection.

2.5.2 Read and Program/Erase Cycle

- Read: No Limitation
- Program/Erase: 5,000,000 times  
(Estimated on reference to Doc No.SM070001)

2.5.3 MTBF (Mean Time Between Failure)

- 2,000,000 hours  
(Estimated on reference to Doc No.SM070002)

2.5.4 Power Cycle

- The Power Cycling is tested to 5000 loop. => “Pass”

2.6 Compliance Specifications

- CE
- FCC

※ Note: Please contact your closest CSS office for other certificate information.

### 3. Function

#### 3.1 Pin Signal Assignment

- The signals assigned for CF Card applications are described in Figure 4 and Table 2;



Figure 4: CompactFlash

Connector

Storage Card Signal

Table 2 : Compact Flash Storage Card Pin Assignment

Pin NO.	PC Card Memory Mode		PC Card I/O Mode		True IDE Mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CS0	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATA SEL	I
10	A9	I	A9	I	A9	I
11	A8	I	A8	I	A8	I
12	A7	I	A7	I	A7	I
13	VCC	—	VCC	—	VCC	—
14	A6	I	A6	I	A6	I
15	A5	I	A5	I	A5	I
16	A4	I	A4	I	A4	I
17	A3	I	A3	I	A3	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOIS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	-CE2	I	-CE2	I	-CS1	I
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD HSTROBE -HDMARDY	I
35	-IOWR	I	-IOWR	I	-IOWR STOP	I
36	-WE	I	-WE	I	-WE	I
37	READY	O	-IREQ	O	INTRQ	O
38	VCC	—	VCC	—	VCC	—
39	-CSEL	I	-CSEL	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	-RESET	I

Pin NO.	PC Card Memory Mode		PC Card I/O Mode		True IDE Mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O
42	-WAIT	O	-WAIT	O	IORDY -DDMARDY DSTROBE	O
43	-INPACK	O	-INPACK	O	DMARQ	O
44	-REG	I	-REG	I	DMACK	I
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	—	GND	—	GND	—

### 3.2 Card Pin Signal Description

**Table 3 : CompactFlash Storage Card Pin Signal Description**

Signal Name	Dir.	Pin No.	Description
A10 - A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the-REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF + Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card , a byte in the card's information structure and its configuration control and status registers.
A10 - A0 (PC Card I/O Mode)			This Signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode)			In True IDE Mode only A [2:0] are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states; while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card / I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1,-CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
-CD1,-CD2 (PC Card Memory Mode)			This signal is the same for all modes.
-CD1,-CD2 (PC Card Memory Mode)			This signal is the same for all modes.

Signal Name	Dir.	Pin No.	Description
-CE1,-CE2 (PC Card I/O Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0,-CE1,-CE2 allows 8 bit hosts to access all data on D0 to D7.
-CE1,-CE2 (PC Card I/O Mode) Card Enable			This Signal is the same as the PC Card Memory Mode signal.
-CS0,-CS1 (True IDE Mode)			In the True IDE Mode -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2,23, 22,21	These lines carry the Data, Commands and Status information between the host and the controller.D00 is the LSB of the Even Byte of the Word.D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This Signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)	–	1,50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.

Signal Name	Dir.	Pin No.	Description
<p>-INPCAK (PC Card Memory Mode)</p> <p>-INPACK (PC Card I/O Mode) Input Acknowledge</p> <p>-DMARQ (True IDE Mode)</p>	O	43	<p>This signal is not used in this mode.</p> <p>The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU.</p> <p>This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer.</p> <p>DMARQ shall not be driven when the device is not selected.</p> <p>While a DMA operation is in progress, -CS0 and-CS1 shall be held negated and the width of the transfers shall be 16 bits.</p> <p>If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode.</p> <p>A host that dose not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE modes as long as this does not prevent proper operation in any mode.</p>
<p>-IORD (PC Card Memory Mode)</p> <p>-IORD (PC Card I/O Mode)</p> <p>-IORD (True IDE Mode) Ultra DMA Protocol Active)</p> <p>-HDMARDY (True IDE Mode – In Ultra DMA Protocol DMA Read)</p> <p>HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)</p>	I	34	<p>This signal is not used in this mode.</p> <p>This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF +Card when the card is configured to use the I/O interface.</p> <p>In True IDE Mode, while Ultra DMA mode DMA read is active, this signal has same function as in PC Card I/O Mode.</p> <p>In True IDE Mode when Ultra DMA mode DMA Read is active, This signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer.</p> <p>In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.</p>

Signal Name	Dir.	Pin No.	Description
-IOWR (PC Card Memory Mode)  -IOWR (PC Card I/O Mode)  -IOWR (True IDE Mode – Except Ultra DMA Protocol)  STOP (True IDE Mode – Ultra DMA Protocol Active)	I	35	This signal is not used in this mode.  The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompcatFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface.  The clocking shall occur on the negative to positive edge of the signal (Trailing edge)  In True IDE Mode, While Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.  In true IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
-OE (PC Card Memory Mode)  -OE (PC Card I/O Mode)  -ATA SEL (True IDE Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.  In PC Card I/O Mode. This signal is used to read the CIS and configuration registers.  To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode)  -IREQ (PC Card I/O Mode)  INTRQ (True IDE Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy.  At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time.  Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled, Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.  I/O Operation - After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as interrupt Request. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt.  In True IDE Mode signal is the active high interrupt Request to the host.

Signal Name	Dir.	Pin No.	Description
<p>-REG (PC Card Memory Mode) Attribute Memory Select</p> <p>-REG (PC Card I/O Mode)</p> <p>-DMACK (True IDE Mode)</p>	I	44	<p>This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.</p> <p>The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.</p> <p>This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to Initiate DMA transfers.</p> <p>While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition.</p> <p>If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host.</p> <p>A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA Mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.</p>
<p>RESET (PC Card Memory Mode)</p> <p>RESET (PC Card I/O Mode)</p> <p>-RESET (True IDE Mode)</p>	I	41	<p>The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception:</p> <p>The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card, Under either of these conditions, the card shall emerge from power-up having completed an initial Reset.</p> <p>The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.</p> <p>This signal is the same as the PC Card Memory Mode signal.</p> <p>In the True IDE Mode, This input pin is the active low hardware reset from the host.</p>
<p>VCC (PC Card Memory Mode)</p> <p>VCC (PC Card I/O Mode)</p> <p>VCC (True IDE Mode)</p>	–	13,38	<p>+5V +3.3V power.</p> <p>This signal is the same for all modes.</p> <p>This signal is the same for all modes.</p>
<p>-VS1 -VS2 (PC Card Memory Mode)</p> <p>-VS1 -VS2 (PC Card I/O Mode)</p> <p>-VS1 -VS2 (True IDE Mode)</p>	O	33,40	<p>Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.</p> <p>This signal is the same for all modes.</p> <p>This signal is the same for all modes.</p>

Signal Name	Dir.	Pin No.	Description
-WAIT (PC Card Memory Mode)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card Memory Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE mode – Except Ultra DMA mode)			In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
-DDMARDY (True IDE mode – Ultra DMA Write mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is ready to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer.
-DSTROBE (True IDE mode – Ultra DMA Read mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host, The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	Memory Mode - The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation - When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

### 3.3 Card Capacity and Cylinder, Head, Sector

The table 4 show various capacities available for AC73 series, if your platform does not support auto-detection function or AC73 series is not identified, we advice can following below Cylinders, Heads, Sectors number to setting your platform.

**Table 4 : Card Capacity and Cylinder, Head, Sector**

Unformatted Disk Capacity	No. of Cylinders	No. of Heads	No. of Sectors	Disk Total Sector
128MB	480	16	32	245760
256MB	960	16	32	491520
512MB	975	16	63	982800
1GB	1950	16	63	1965600
2GB	3900	16	63	3931200
4GB	7801	16	63	7863408
8GB	15603	16	63	15727824

## 4. Operation Specification

### 4.1 Absolute Maximum Ratings

Table 5: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	VCC	-0.3 ~ +5.6	V
Input voltage	Vin	-0.3 ~ +5.6	V

(Referenced to GND)

### Electric characteristics

Vcc=3.14V~5.5V

Item	Symbol	Value			Unit	Measuring conditions
		Min.	Standard	Max.		
Input voltage (TTL level)	V <sub>IH</sub>	2.0	-	*1	V	
	V <sub>IL</sub>	-	-	0.7	V	
Output voltage	V <sub>OH</sub>	2.2	-	*2	V	I <sub>OH</sub> =-2mA~ -24mA
	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> =2mA~ 24mA

### 4.2 Series termination required for Ultra DMA operation

Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes, Table 6 describes typical values for series termination at the host and the device.

Table 6: Typical Series Termination for Ultra DMA

Signal	Host Termination	Device Termination
-IORD (-HDMARDY, HSTROBE)	22 ohm	82 ohm
-IOWR ( STOP)	22 ohm	82 ohm
-CS0, -CS1	33 ohm	82 ohm
A00, A01, A02	33 ohm	82 ohm
-DMACK	22 ohm	82 ohm
D15 through D00	33 ohm	33 ohm
DMARQ	82 ohm	22 ohm
INTRQ	82 ohm	22 ohm
IORDY (-DDMARDY, DSTROBE)	82 ohm	22 ohm
-RESET	33 ohm	82 ohm

Note – Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. Shows signals also requiring a pull-up or pull down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.

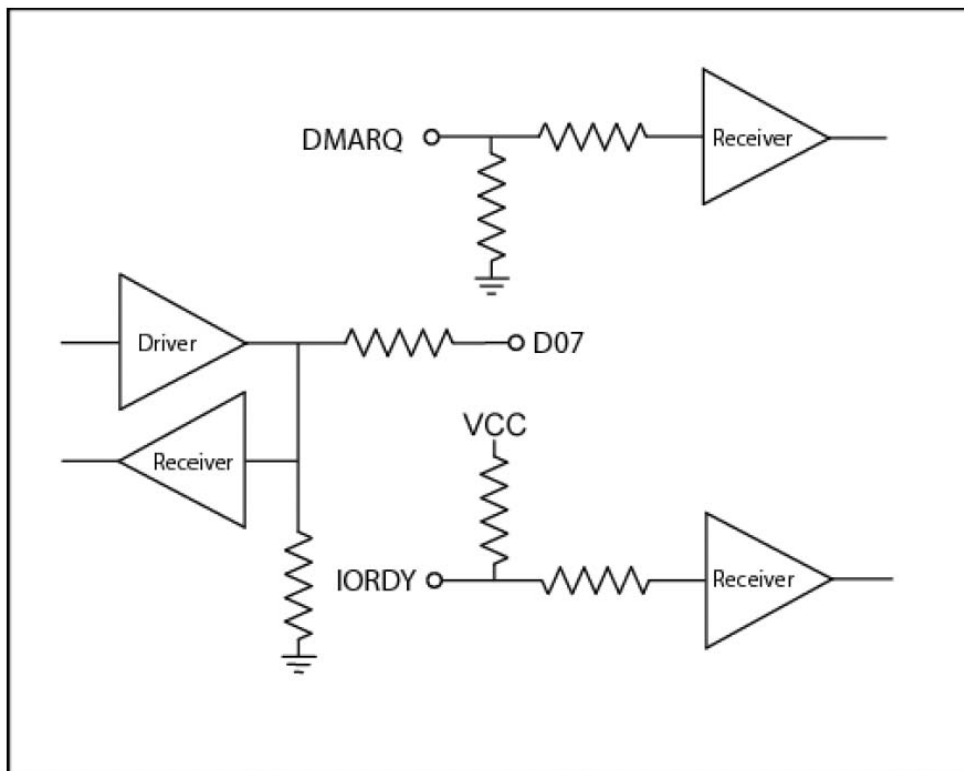


Figure 5: Ultra DMA termination with Pull-up or Pull down Example

### 4.3 Attribute Memory Read Timing Specification

Attribute Memory access time is define as 300 ns. Detailed timing specs are shown in Table 7.

Table 7: Attribute Memory Read Timing

Speed Version			300 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Read Cycle Time	$t_{c(R)}$	$t_{AVAV}$	300	
Address Access Time	$t_{a(A)}$	$t_{AVQV}$		300
Card Enable Access Time	$t_{a(CE)}$	$t_{ELQV}$		300
Output Enable Access Time	$t_{a(OE)}$	$t_{GLQV}$		150
Output Disable Time from CE	$t_{dis(CE)}$	$t_{EHQZ}$		100
Output Disable Time from OE	$t_{dis(OE)}$	$t_{GHQZ}$		100
Address Setup Time	$t_{su(A)}$	$t_{AVGL}$	30	
Output Enable Time from CE	$t_{en(CE)}$	$t_{ELQNZ}$	5	
Output Enable Time from OE	$t_{en(OE)}$	$t_{GLQNZ}$	5	
Data valid from Address Change	$t_{v(A)}$	$t_{AXQX}$	0	

Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card to the system. The  $-\text{CE}$  signal or both the  $-\text{OE}$  signal and the  $-\text{WE}$  signal shall be de-asserted between consecutive cycle operations.

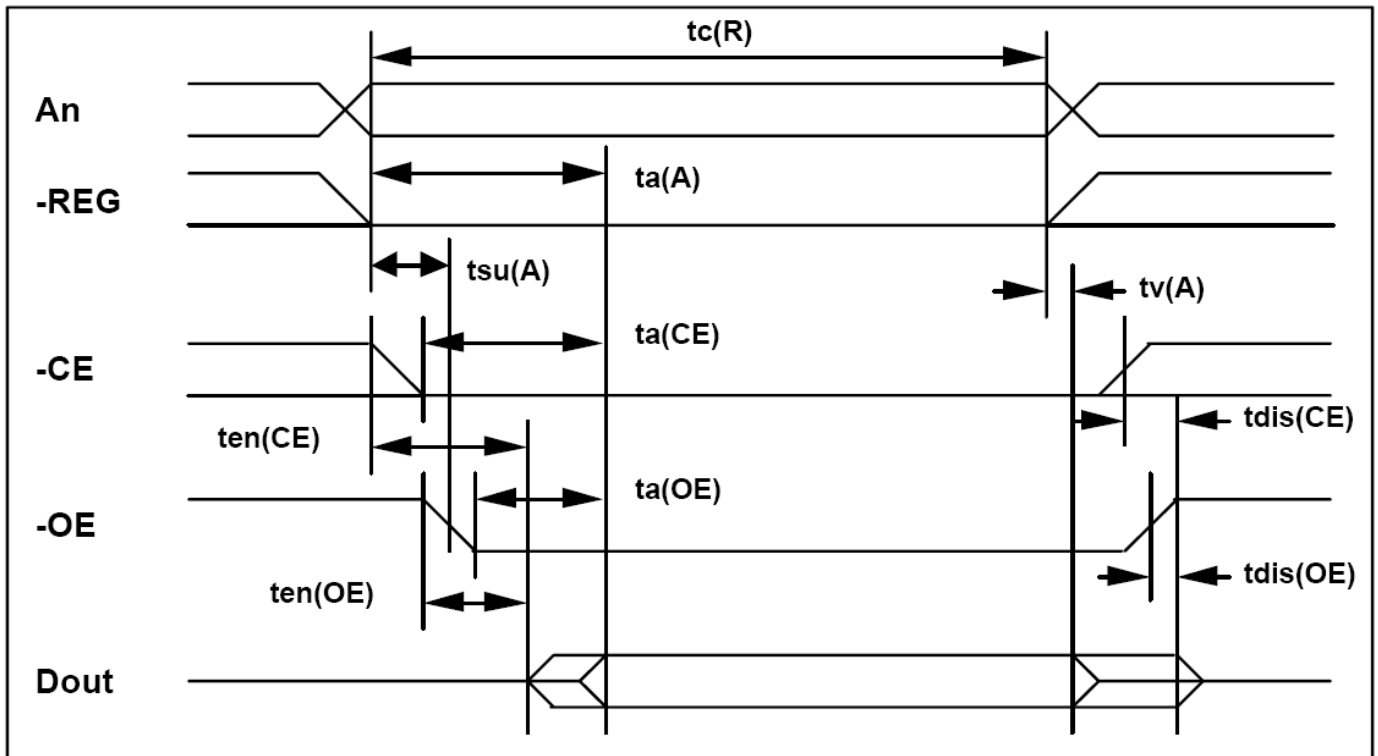


Figure 6: Attribute Memory Read Timing Diagram

4.4 Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250ns. Detailed timing specifications are shown in Table 8.

Table 8: Configuration Register (Attribute Memory) Write Timing

Speed Version			250 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Write Cycle Time	$t_c(W)$	$t_{AVAV}$	250	
Write Pulse Width	$t_w(WE)$	$t_{WLWH}$	150	
Address Setup Time	$t_{su}(A)$	$t_{AVWL}$	30	
Write Recovery Time	$t_{rec}(WE)$	$t_{WMAX}$	30	
Data Setup Time for WE	$T_{su}(D-WEH)$	$t_{DVWH}$	80	
Data Hold Time	$t_h(D)$	$t_{WMDX}$	30	

Note: All times are in nanoseconds. Din signifies data provide by the system to the CompactFlash Storage Card.

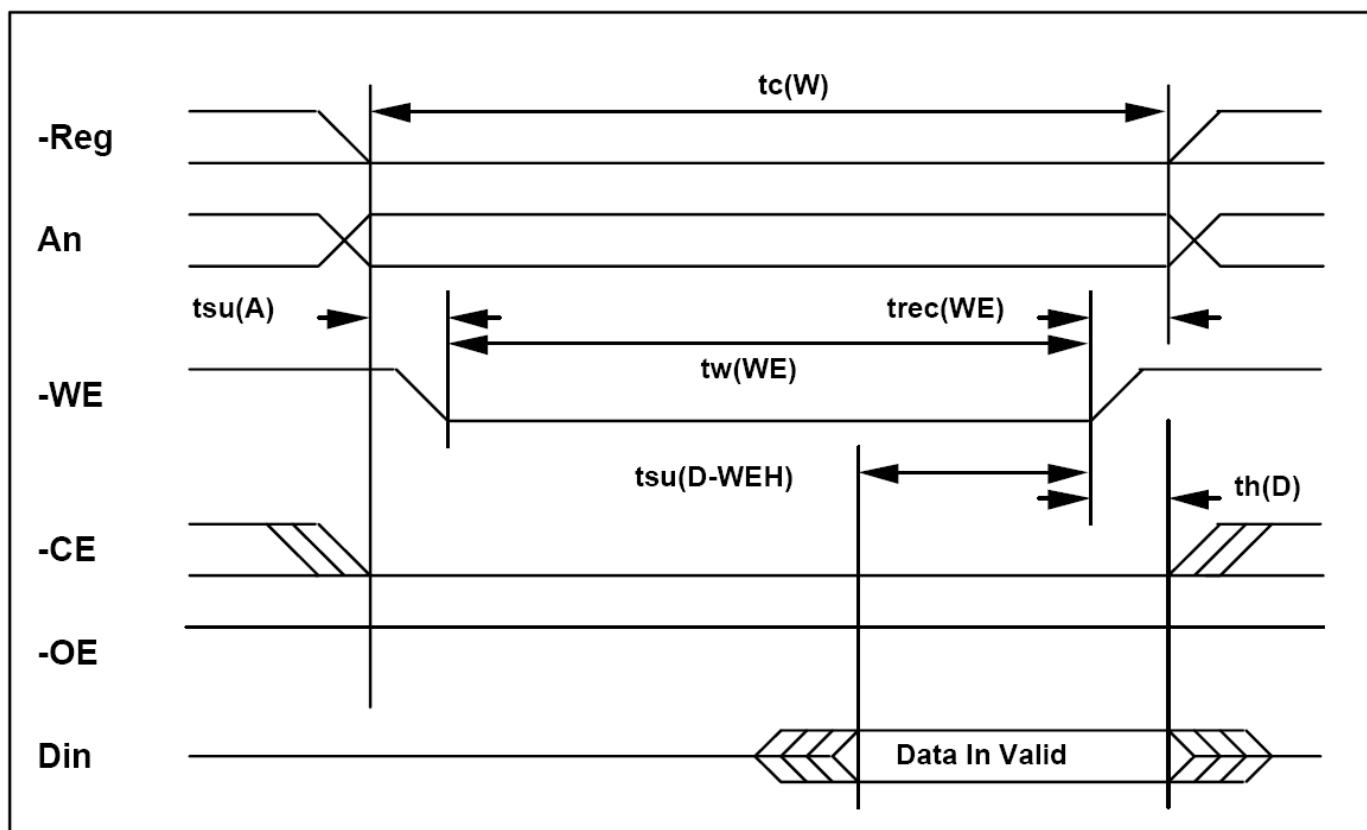


Figure 7: Configuration Register (Attribute Memory) Write Timing Diagram

4.5 Common Memory Read Timing Specification

Table 9 : Common Memory Read Timing

Cycle Time Mode:			250 ns		120 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125		60
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60
Address Setup Time	tsu(A)	tAVGL	30		15	
Address Hold Time	th(A)	tGHAX	20		15	
CE setup Before OE	tsu(CE)	tELGL	0		0	
CE Hold following OE	th(CE)	tGHEH	20		15	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0
Wait Width Time <sup>2</sup>	tw(WT)	tWTLWTH		350		350

Note:  
 1) –WAIT is not supported in this mode.  
 2) The maximum load on –WAIT is 1 LSTTL with 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card to the system. The –WAIT signal may be ignored if the –OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally less in this specification.

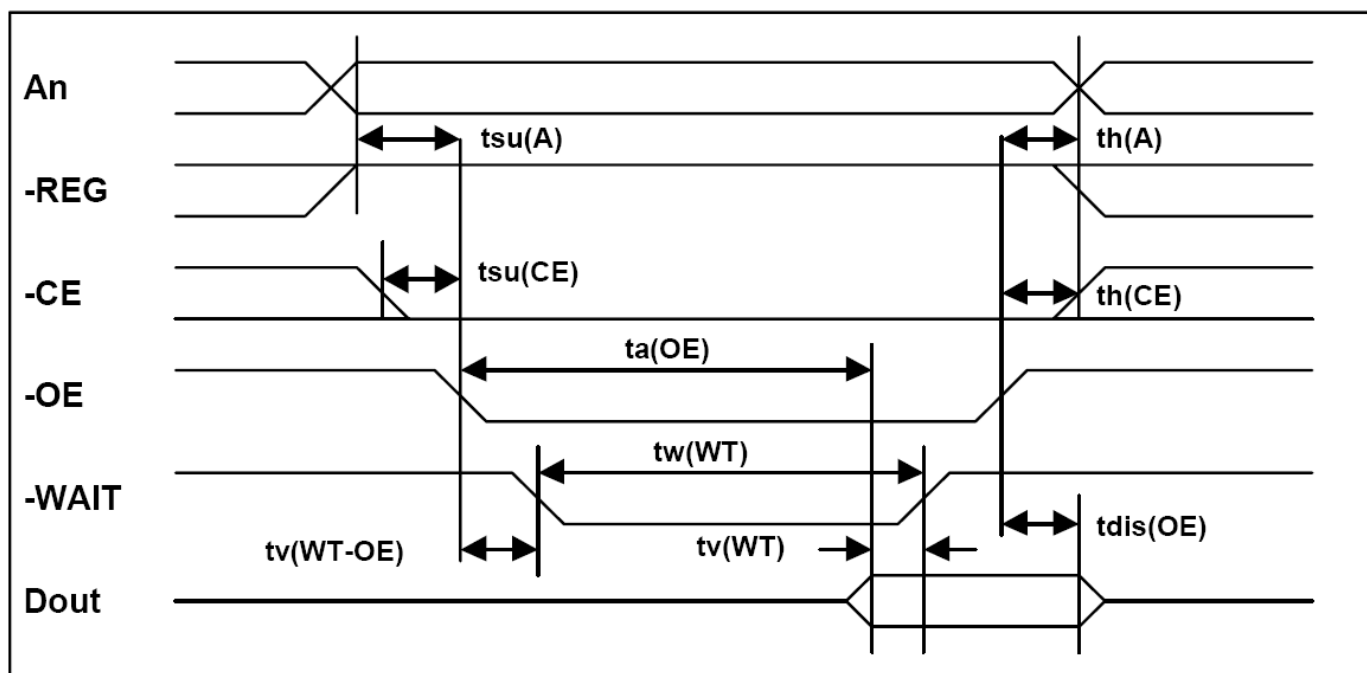


Figure 8: Common Memory Read Timing Diagram

#### 4.6 Common Memory Write Timing Specification

Table 10 : Common Memory Write Timing

Cycle Time Mode:			250 ns		120 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before WE	tsu (D-WEH)	tDVWH	80		50	
Data Hold following WE	th(D)	tWMDX	30		15	
WE Pulse Width	tw(WE)	tWLWH	150		70	
Address Setup Time	tsu(A)	tAVWL	30		15	
CE Setup before WE	tsu(CE)	tELWL	0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15	
Address Hold Time	th(A)	tGHAX	20		15	
CE Hold following WE	th(CE)	tGHEH	20		15	
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35		35
WE High from Wait Release	tv(WT)	tWTHWH	0		0	
Wait Width Time <sup>2</sup>	tw(WT)	tWTLWTH		350		350

Note:  
 1) -WAIT is not supported in this mode.  
 2) The maximum load on -WAIT is 1 LSTTL with 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally in this specification.

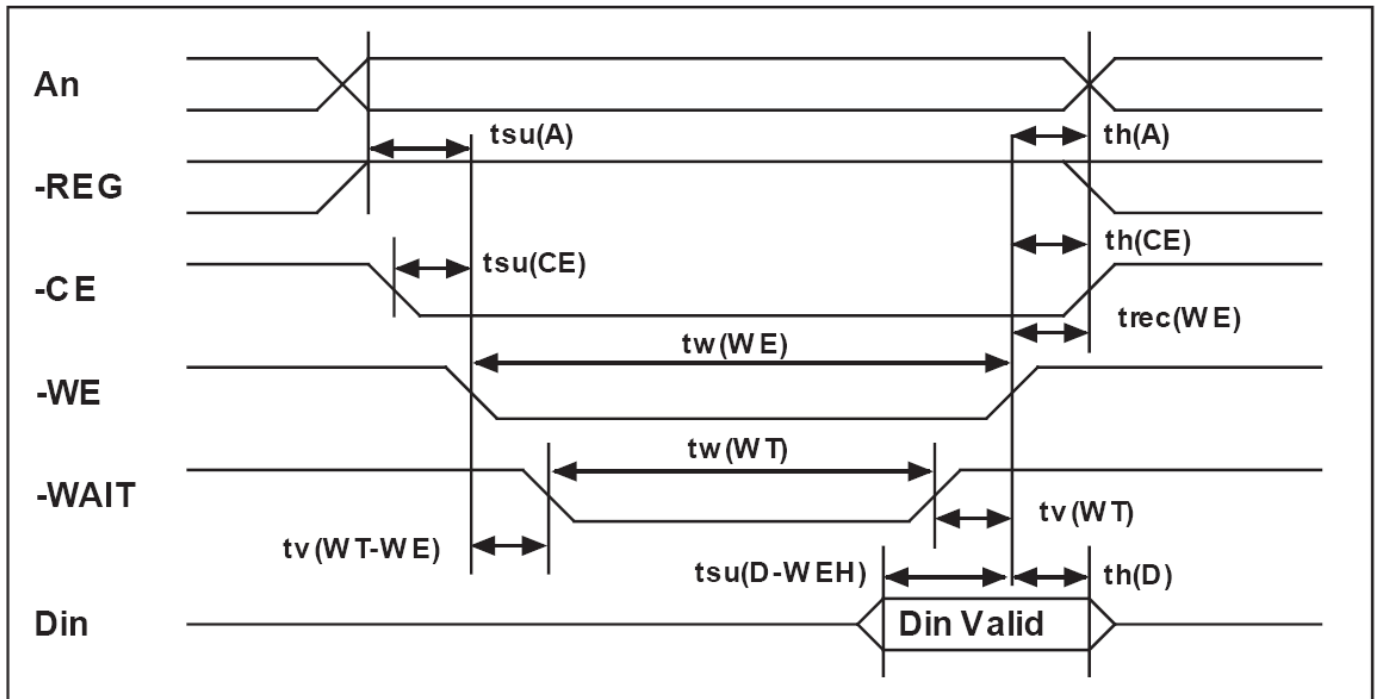


Figure 9: Common Memory Write Timing Diagram

4.7 I/O Input (Read) Timing Specification

Table 11 : I/O Read Timing

Cycle Time Mode:			250 ns		120 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100		50
Data Hold Following IORD	th(IORD)	tIGHQX	0		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5		5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		0	
INPACK Delay Falling from IORD <sup>3</sup>	tdfINLACK(IORD)	tIGLIAL	0	45	0	na <sup>1</sup>
INPACK Delay Rising from IORD <sup>3</sup>	tdrINPACK(IORD)	tIGHIAH		45		na <sup>1</sup>
IOIS16 Delay Falling from Address <sup>3</sup>	tdfIOIS16	tAVISL		35		na <sup>1</sup>
IOIS16 Delay Rising from Address <sup>3</sup>	tdrIOIS16(ADR)	tAVISH		35		na <sup>1</sup>
Wait Delay Falling from IORD <sup>3</sup>	tdWT(IORD)	tIGLWTL		35		35
Data Delay from Wait Rising <sup>3</sup>	td(WT)	tWTHQV		0		0
Wait Width Time <sup>3</sup>	tw(WT)	tWTLWTH		350		350

Notes:

- 1) -IOIS16 and -INPACK are not supported in this mode.
- 2) -WAIT is not supported in this mode.
- 3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall be met. Dout signifies data provided by the CompactFlash Storage Card to the system. Wait Width time meets PCMCIA specification of 12us but is intentionally less in this spec.

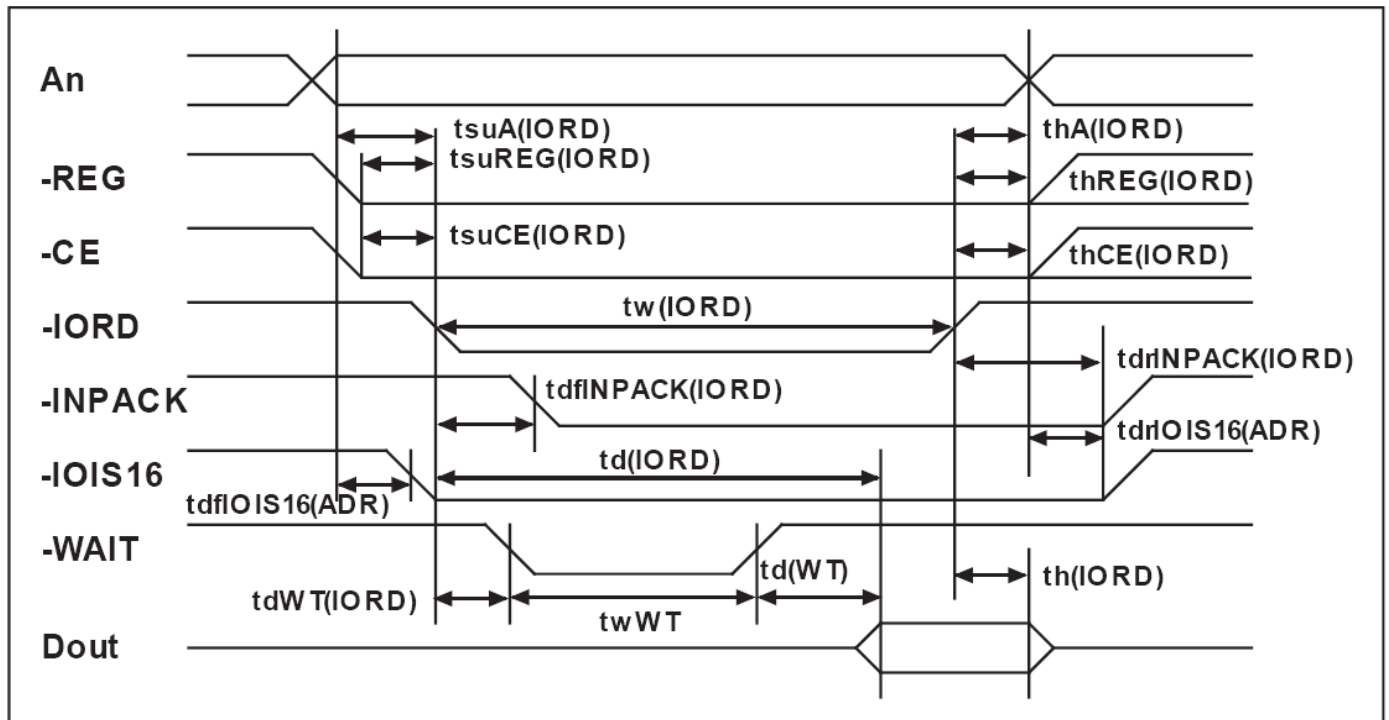


Figure 10: I/O Read Timing Diagram

4.8 I/O Input (Write) Timing Specification

Table 12 : I/O Write Timing

Cycle Time Mode:			250 ns		120 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20	
Data Hold Following IOWR	th(IOWR)	tIWHDX	30		10	
IOWR Width Time	tw(IOWR)	tIWLWH	165		70	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20	
CE Setup before IOWR	tsuCE (IOWR)	tELIWL	5		5	
CE Hold following IOWR	thCE (IOWR)	tIWHEH	20		20	
REG Setup before IOWR	tsuREG (IOWR)	tRGLIWL	5		5	
REG Hold following IOWR	thREG (IOWR)	tIWHRGH	0		0	
IOIS16 Delay Falling From Address <sup>3</sup>	tdfIOIS16 (ADR)	tAVISL		35		na <sup>1</sup>
IOIS16 Delay Rising from Address <sup>3</sup>	tdrIOIS16 (ADR)	tAVISH		35		na <sup>1</sup>
Wait Delay Falling from IOWR <sup>3</sup>	tdWT (IOWR)	tIWLWTL		35		35
IOWR high from Wait high <sup>3</sup>	tdrIOWR (WT)	tWTJIWH	0		0	
Wait Width Time <sup>3</sup>	tw(WT)	tWTLWTH		350		350

Notes:

- 1) -IOIS16 and -INPACK are not supported in this mode.
- 2) -WAIT is not supported in this mode.
- 3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall be met. Din signifies data provided by the system to the 12us but is intentionally less in this specification.

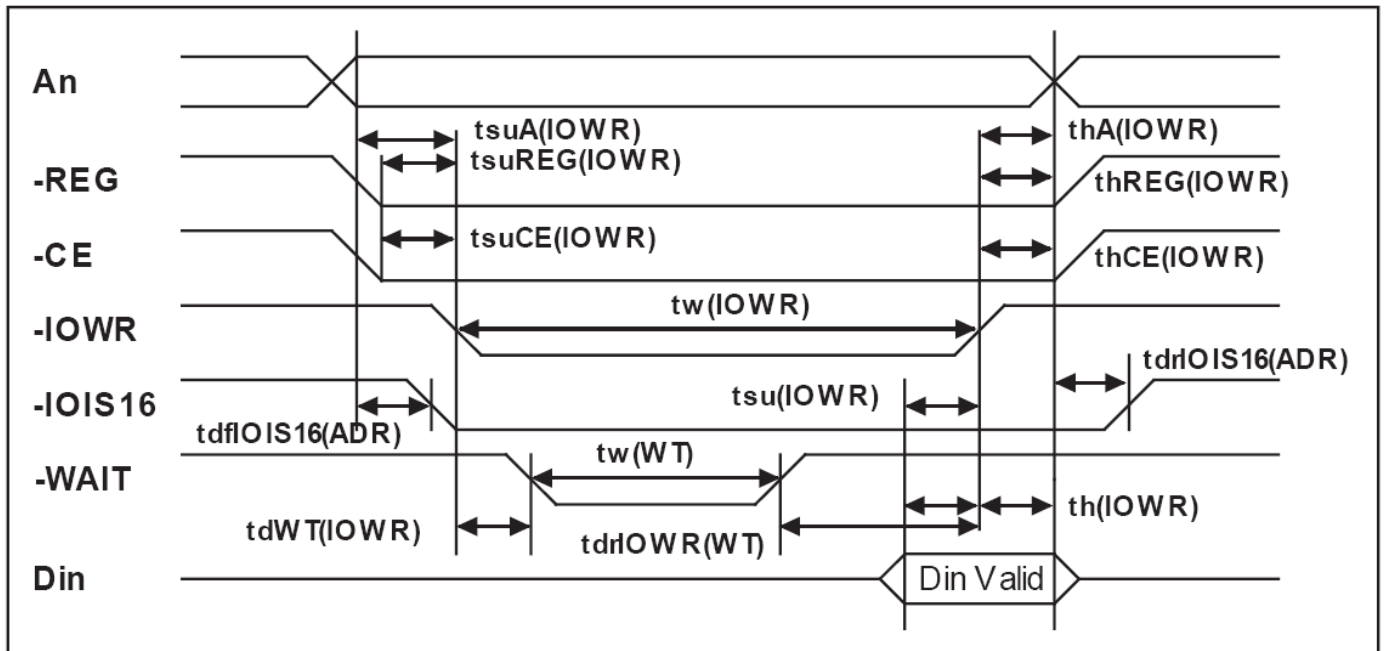


Figure 11: I/O Write Timing Diagram

**4.9 True IDE PIO Mode Read/Write Timing Specification**

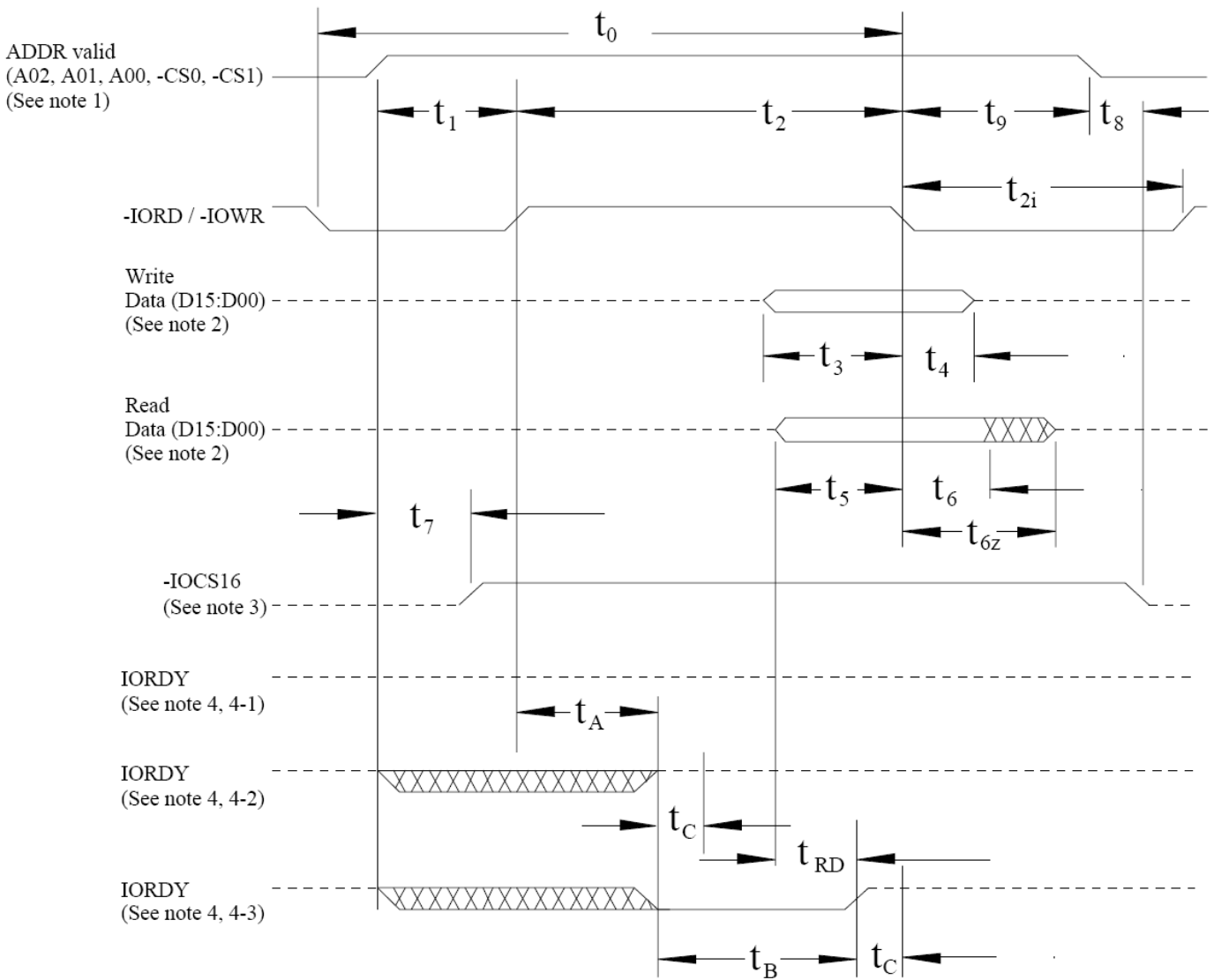
The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the  $\text{-IOR}$ , the  $\text{-IOW}$  and the  $\text{-IOCS16}$  signals are shown in the diagram inverted from their electrical states on the bus.

**Table 13: True IDE PIO Mode Read/Write Timing**

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
t0	Cycle Time (min)	600	383	240	180	120	1
t1	Address Valid to $\text{-IOR}$ / $\text{-IOW}$ setup (min)	70	50	30	30	25	
t2	$\text{-IOR}$ / $\text{-IOW}$ (min)	165	125	100	80	70	1
t2	$\text{-IOR}$ / $\text{-IOW}$ (min) Register (8bit)	290	290	290	80	70	1
t2i	$\text{-IOR}$ / $\text{-IOW}$ recovery time(min)	-	-	-	70	25	1
t3	$\text{-IOW}$ data setup (min)	60	45	30	30	20	
t4	$\text{-IOW}$ data hold (min)	30	20	15	10	10	
t5	$\text{-IOR}$ data setup(min)	50	35	20	20	20	
t6	$\text{-IOR}$ data hold (min)	5	5	5	5	5	
t6Z	$\text{-IOR}$ data tristate (max)	30	30	30	30	30	2
t7	Address valid to $\text{-IOCS16}$ assertion (max)	90	50	40	n/a	n/a	4
t8	Address valid to $\text{-IOCS16}$ released (max)	60	45	30	n/a	n/a	4
t9	$\text{-IOR}$ / $\text{-IOW}$ to address valid hold	20	15	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
tC	IORDY assertion to release(max)	5	5	5	5	5	

Note:  
 All timings are in nanoseconds. The maximum load on  $\text{-IOCS16}$  is 1 LSTTL with a 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from  $\text{-IORDY}$  high to  $\text{-IOR}$  high is 0 nsec, but minimum  $\text{-IOR}$  width shall still be met.

- 1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time, The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.
- 2) This Parameter Specifies the time from the negation edge of  $\text{-IOR}$  to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).
- 3) The delay from the activation of  $\text{-IOR}$  or  $\text{-IOW}$  until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of  $\text{-IOR}$  or  $\text{-IOW}$ , then t5 shall be met and tRD is not applicable. If the Compact Flash Storage Card is Driving IORDY negated at the time tA after the activation of  $\text{-IOR}$  or  $\text{-IOW}$ , then tRD shall be met and t5 is not applicable.
- 4) t7 and t8 apply only to modes0, 1 and 2. For other modes, this signal is not valid.
- 5) IORDY is not supported in this mode.



Notes:

- (1) Device address consists of -CS0, -CS1, and A[02::00]
- (2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
- (3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
- (4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after  $t_A$  from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
  - (4-1) Device never negates IORDY: No wait is generated.
  - (4-2) Device starts to drive IORDY low before  $t_A$ , but causes IORDY to be asserted before  $t_A$ : No wait generated.
  - (4-3) Device drives IORDY low before  $t_A$ : wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for  $t_{RD}$  before causing IORDY to be asserted.

**ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.**

Figure 12: True IDE PIO Mode Timing Diagram

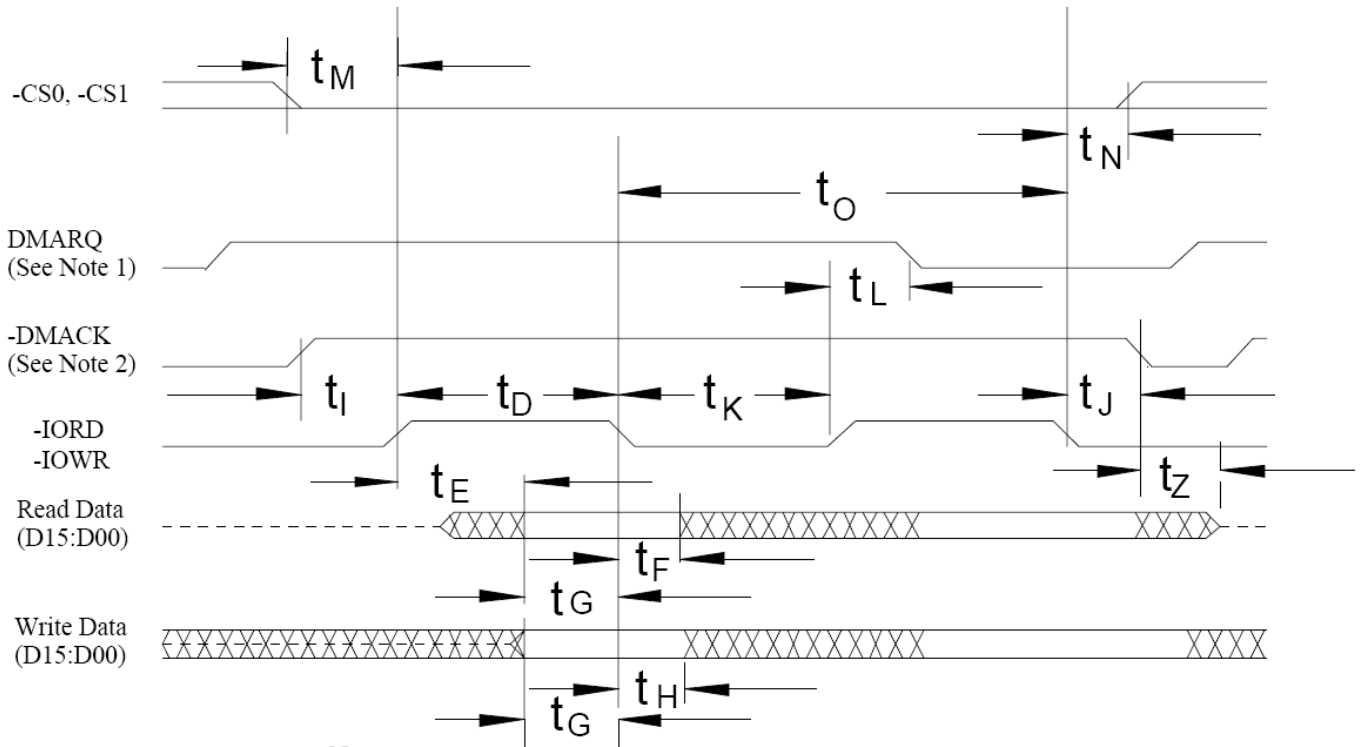
**4.10 True IDE Multiword DMA Mode Read/Write Timing Specification**

The timing diagram for true IDE DMA mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the  $\text{-IOR\!D}$ , the  $\text{-IOWR}$  and the  $\text{-IOCS16}$  signals are shown in the diagram inverted from their electrical states on the bus.

**Table 14: True IDE Multiword DMA mode Read/Write Timing**

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Note
$t_O$	Cycle time (min)	480	150	120	1
$t_D$	$\text{-IOR\!D}/\text{-IOWR}$ asserted width (min)	215	80	70	1
$t_E$	$\text{-IOR\!D}$ data access (max)	150	60	50	
$t_F$	$\text{-IOR\!D}$ data hold(min)	5	5	5	
$t_G$	$\text{-IOR\!D}/\text{-IOWR}$ data setup(min)	100	30	20	
$t_H$	$\text{-IOWR}$ data hold(min)	20	15	10	
$t_I$	DMACK to $\text{-IOR\!D}/\text{-IOWR}$ setup (min)	0	0	0	
$t_J$	$\text{-IOR\!D}/\text{-IOWR}$ to $\text{-DMACK}$ hold (min)	20	5	5	
$t_{KR}$	$\text{-IOR\!D}$ negated width (min)	50	50	25	1
$t_{KW}$	$\text{-IOWR}$ negated width (min)	215	50	25	1
$t_{LR}$	$\text{-IOR\!D}$ to DMARQ delay (max)	120	40	35	
$t_{LW}$	$\text{-IOWR}$ to DMARQ delay (max)	40	40	35	
$t_M$	CS(1:0) valid to $\text{-IOR\!D}$ / $\text{-IOWR}$	50	30	25	
$t_N$	CS(1:0) hold	15	10	10	
$t_Z$	$\text{-DMACK}$	20	25	25	

Note:  
 1)  $t_O$  is the minimum total cycle time and  $t_D$  the minimum command active time, while  $t_{KR}$  and  $t_{KW}$  are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of  $t_O$ ,  $t_D$ ,  $t_{KR}$ , and  $t_{KW}$  shall be met. The minimum total cycle time requirement is greater than the sum of  $t_D$  and  $t_{KR}$  or  $t_{KW}$  for input and output cycles respectively. This mean a host implementation can lengthen either or both of  $t_D$  and either of  $t_{KR}$ , and  $t_{KW}$  as needed to ensure that  $t_O$  is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.



Notes:

- (1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
- (2) This signal may be negated by the host to suspend the DMA transfer in progress.

**ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.**

**Figure 13: True IDE Multiword DMA Read/Write Timing Diagram**

### 4.11 True IDE Ultra DMA Mode Read/Write Timing Specification

#### 4.11.1 Ultra DMA Data Transfers Timing

Table 15 and Table 16 define the timings associated with all phases of Ultra DMA bursts.

**Table 15: Ultra DMA Data Burst Timing Requirements**

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		Measurement location (See Note 2)
	Min	Max	Min	Max	Min	Max	
t <sub>CYCTYP</sub>	240		160		120		Sender
t <sub>CYC</sub>	112		73		54		Note 3
t <sub>2CYC</sub>	230		153		115		Sender
t <sub>DS</sub>	15.0		10.0		7.0		Recipient
t <sub>DH</sub>	5.0		5.0		5.0		Recipient
t <sub>DVS</sub>	70.0		48.0		31.0		Sender
t <sub>DVH</sub>	6.2		6.2		6.2		Sender
t <sub>CS</sub>	15.0		10.0		7.0		Device
t <sub>CH</sub>	5.0		5.0		5.0		Device
t <sub>CVS</sub>	70.0		48.0		31.0		Host
t <sub>CVH</sub>	6.2		6.2		6.2		Host
t <sub>ZFS</sub>	0		0		0		Device
t <sub>DZFS</sub>	70.0		48.0		31.0		Sender
t <sub>FS</sub>		230		200		170	Device
t <sub>LI</sub>	0	150	0	150	0	150	Note 4
t <sub>MLI</sub>	20		20		20		Host
t <sub>UI</sub>	0		0		0		Host
t <sub>AZ</sub>		10		10		10	Note 5
t <sub>ZAG</sub>	20		20		20		Host
t <sub>ZAD</sub>	0		0		0		Device
t <sub>ENV</sub>	20	70	20	70	20	70	Host
t <sub>RFS</sub>		75		70		60	Sender
t <sub>RP</sub>	160		125		100		Recipient
t <sub>IORDYZ</sub>		20		20		20	Device
t <sub>ZIORDY</sub>	0		0		0		Device
t <sub>ACK</sub>	20		20		20		Host
t <sub>SS</sub>	50		50		50		Sender

- Note:
- 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5V.
  - 2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t<sub>RFS</sub>, both STROBE and -DMARDY transitions are measured at the sender connector.
  - 3) The parameter t<sub>CYC</sub> shall be measured at the recipient's connector farthest from the sender.
  - 4) The parameter t<sub>LI</sub> shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
  - 5) The parameter t<sub>AZ</sub> shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a turnaround.
  - 6) See the AX Timing requirements in Table 18: Ultra DMA AC Signal Requirements.

**Table 16: Ultra DMA Data Burst Timing Descriptions**

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
$t_{CYC}$	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
$t_{2CYC}$	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
$t_{DS}$	Data setup time at recipient (from data valid until STROBE edge)	2, 5
$t_{DH}$	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
$t_{DVS}$	Data valid setup time at sender (from data valid until STROBE edge)	3
$t_{DVH}$	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
$t_{CS}$	CRC word setup time at device	2
$t_{CH}$	CRC word hold time device	2
$t_{CVS}$	CRC word valid setup time at host (from CRC valid until –DMACK negation)	3
$t_{CVH}$	CRC word valid hold time at sender (from –DMACK negation until CRC may become invalid)	3
$t_{ZFS}$	Time from STROBE output released-to-driving until the first transition of critical timing	
$t_{DZFS}$	Time from data output released-to driving until the first transition of critical timing	
$t_{FS}$	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
$t_{LI}$	Limited interlock time	1
$t_{MLI}$	Interlock time with minimum	1
$t_{UI}$	Unlimited interlock time	1
$t_{AZ}$	Maximum time allowed for output drivers to release (from asserted or negated)	
$t_{ZAG}$	Minimum delay time required for output	
$t_{ZAD}$	Drives to assert or negate (from released)	
$t_{ENV}$	Envelope time(from –DMACK to STOP and –HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
$t_{RFS}$	Ready-to-final-STROBE time(no STROBE edges shall be sent this long after negation of –DMARDY)	
$t_{RP}$	Ready to pause time (that recipient shall wait to pause after negating –DMARDY)	
$t_{IORDYZ}$	Maximum time before releasing IORDY	
$t_{ZIORDY}$	Minimum time before driving IORDY	4
$t_{ACK}$	Setup and hold times for –DMACK (before assertion or negation)	
$t_{SS}$	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Note:

- 1) The parameters  $t_{UI}$ ,  $t_{MLI}$  (in Figure 14: Ultra DMA Data-In Burst Device Termination Timing and Figure 15: Ultra DMA Data-in Burst Host Termination Timing), and  $t_{LI}$  indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.  $t_{UI}$  is an unlimited interlock that has no maximum time value.  $t_{MLI}$  is a limited time-out that has a defined minimum.  $t_{LI}$  is a limited time-out that has a defined maximum.
- 2) 80-conductor cabling shall be required in order to meet setup ( $t_{DS}$ ,  $t_{CS}$ ) and hold ( $t_{DH}$ ,  $t_{CH}$ ) times in modes greater than 3) Timing for  $t_{DVS}$ ,  $t_{DVH}$ ,  $t_{CVS}$  and  $t_{CVH}$  shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
- 4) For all modes the parameter  $t_{ZIORDY}$  may be greater than  $t_{ENV}$  due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
- 5) The parameters  $t_{DS}$  and  $t_{DH}$  for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for  $t_{DS}$  and  $t_{DH}$  for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

**Table 17: Ultra DMA Sender and Recipient IC Timing Requirements**

Name	Comments	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)	
		Min	Max	Min	Max	Min	Max
t <sub>DSIC</sub>	Recipient IC data setup time (from data valid until STROBE edge) (see note2)	14.7		9.7		6.8	
t <sub>DHIC</sub>	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)	4.8		4.8		4.8	
t <sub>DVSIc</sub>	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)	72.9		50.9		33.9	
t <sub>DVHIc</sub>	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)	9.0		9.0		9.0	

- Note:
- 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
  - 2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling at t<sub>DSIC</sub> and t<sub>DHIC</sub> timing (as measured through 1.5 V).
  - 3) The parameters t<sub>DVSIc</sub> and t<sub>DVHIc</sub> shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

**Table 18: Ultra DMA AC Signal Requirements**

Name	Comment	Min[V/ns]	Max[V/ns]	Notes
S <sub>RISE</sub>	Rising Edge Slew Rate for any signal		1.25	1
S <sub>FALL</sub>	Falling Edge Slew Rate for any signal		1.25	1

- Note:
- 1) The Sender shall be tested while driving an 18inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point in on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

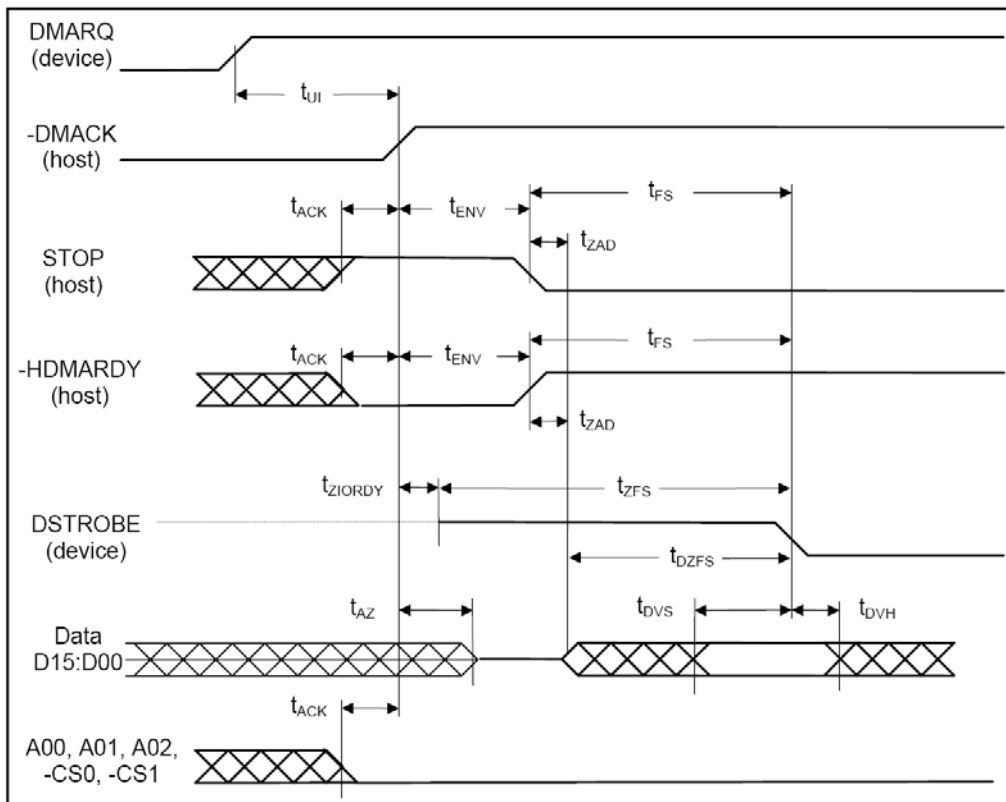
The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1pF, >100 Kohm, 1 GHz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

**4.11.2 Initiating an Ultra DMA Data-In Burst**

- a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 14: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.
- b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:
- c) The host shall keep –DMACK in the negated state before an Ultra DMA burst is initiated.
- d) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.
- e) Steps(c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
- f) The host shall negate –HDMARDY.

- g) The host shall negate  $\text{-CS0}$ ,  $\text{-CS1}$ ,  $\text{-DA2}$ ,  $\text{-DA1}$ , and  $\text{DA0}$ . The host shall keep  $\text{-CS0}$ ,  $\text{-CS1}$ ,  $\text{DA2}$ ,  $\text{DA1}$ , and  $\text{DA0}$  negated until after negating  $\text{-DMACK}$  at the end of the burst.
- h) Steps(c), (d), and (e) shall have occurred at least  $t_{\text{ACK}}$  before the host asserts  $\text{-DMACK}$ . The host shall keep  $\text{-DMACK}$  asserted until the end of an Ultra DMA burst.
- i) The host shall release  $\text{D}[15:00]$  within  $t_{\text{AZ}}$  after asserting  $\text{-DMACK}$ .
- j) The device may assert  $\text{DSTROBE}$   $t_{\text{ZIORDY}}$  after the host has asserted  $\text{-DMACK}$ . Once the device has driven  $\text{DSTROBE}$  the device shall not release  $\text{DSTROBE}$  until after the host has negated  $\text{-DMACK}$  at the end of an Ultra DMA burst.
- k) The host shall negate  $\text{STOP}$  and assert  $\text{-HDMARDY}$  within  $t_{\text{ENV}}$  after asserting  $\text{-DMACK}$ . After negating  $\text{STOP}$  and asserting  $\text{-HDMARDY}$ , the host shall not change the state of either signal until after receiving the first transition of  $\text{DSTROBE}$  from the device (i.e., after the first data word has been received).
- l) The device shall drive  $\text{D}[15:00]$  no sooner than  $t_{\text{ZAD}}$  after the host has asserted  $\text{-DMACK}$ , negated  $\text{STOP}$ , and asserted  $\text{-HDMARDY}$ .
- m) The device shall drive the first word of the data transfer onto  $\text{D}[15:00]$ . This step may occur when the device first drives  $\text{D}[15:00]$  in step (j).
- n) To transfer the first word of data the device shall negate  $\text{DSTROBE}$  within  $t_{\text{FS}}$  after the host has negated  $\text{STOP}$  and asserted  $\text{-HDMARDY}$ . The device shall negate  $\text{DSTROBE}$  no sooner than  $t_{\text{DVS}}$  after driving the first word of data onto  $\text{D}[15:00]$ .



Notes: The definitions for the  $\text{IORDY}$ : $\text{-DDMARDY}$ : $\text{DSTROBE}$ ,  $\text{-IORD}$ :  $\text{-HDMARDY}$ : $\text{HSTROBE}$ , and  $\text{-IOWR}$ : $\text{STOP}$  signal lines are not in effect until  $\text{DMARQ}$  and  $\text{-DMACK}$  are asserted.

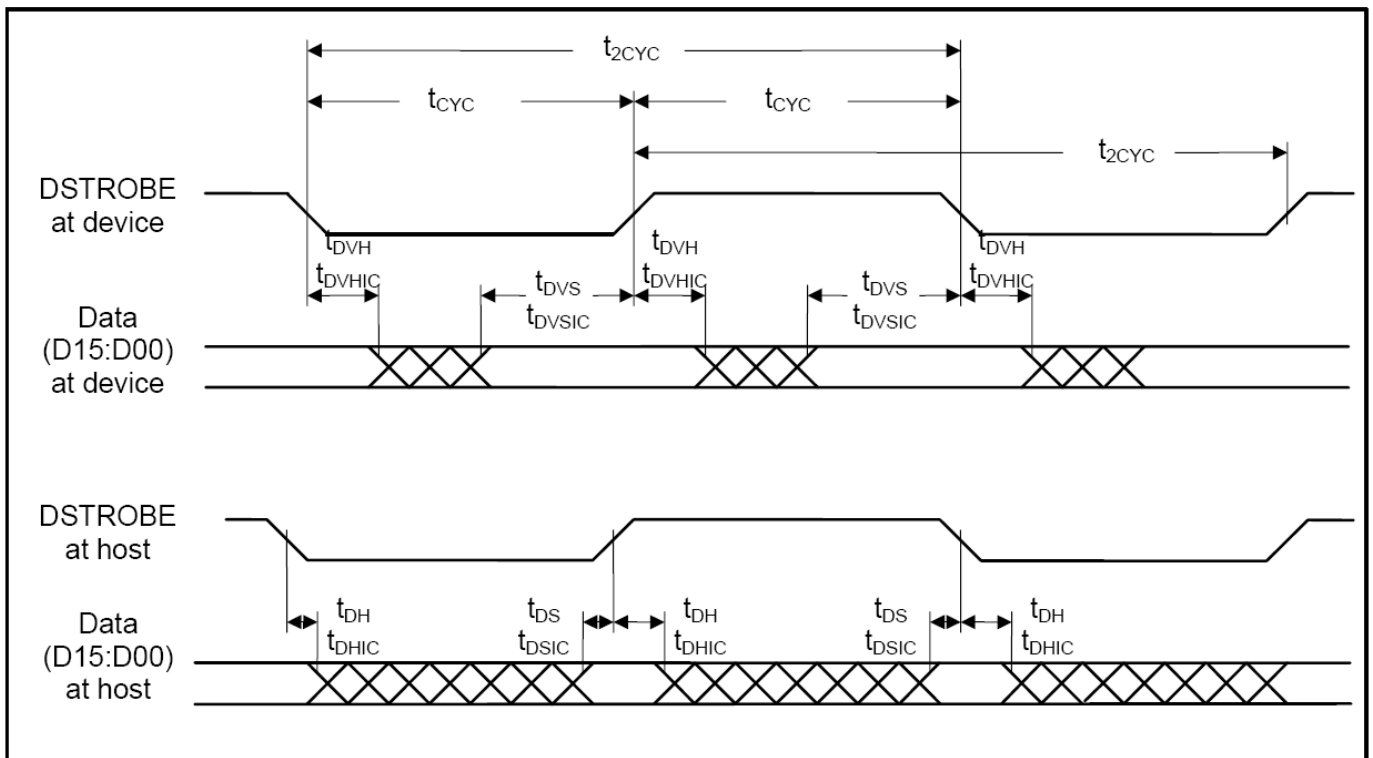
Figure 14: Ultra DMA Data-In Burst Initiation Timing

4.11.3 Sustaining an Ultra DMA data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 15: Sustained Ultra DMA Data-In Burst Timing. The timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The device shall drive a data word onto D[15:00].
- b) The device shall generate a DSTROBE edge to latch the new word no sooner than  $t_{DVS}$  after changing the state of D [15:00]. The device shall generate a DSTROBE edge no more frequently than  $t_{CYC}$  for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than  $2t_{CYC}$  for the selected Ultra DMA mode.
- c) The device shall not change the state of D[15:00] until at least  $t_{DVH}$  after generating a DSTROBE edge to latch the data.
- d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.



Notes: **D[15:00]** and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

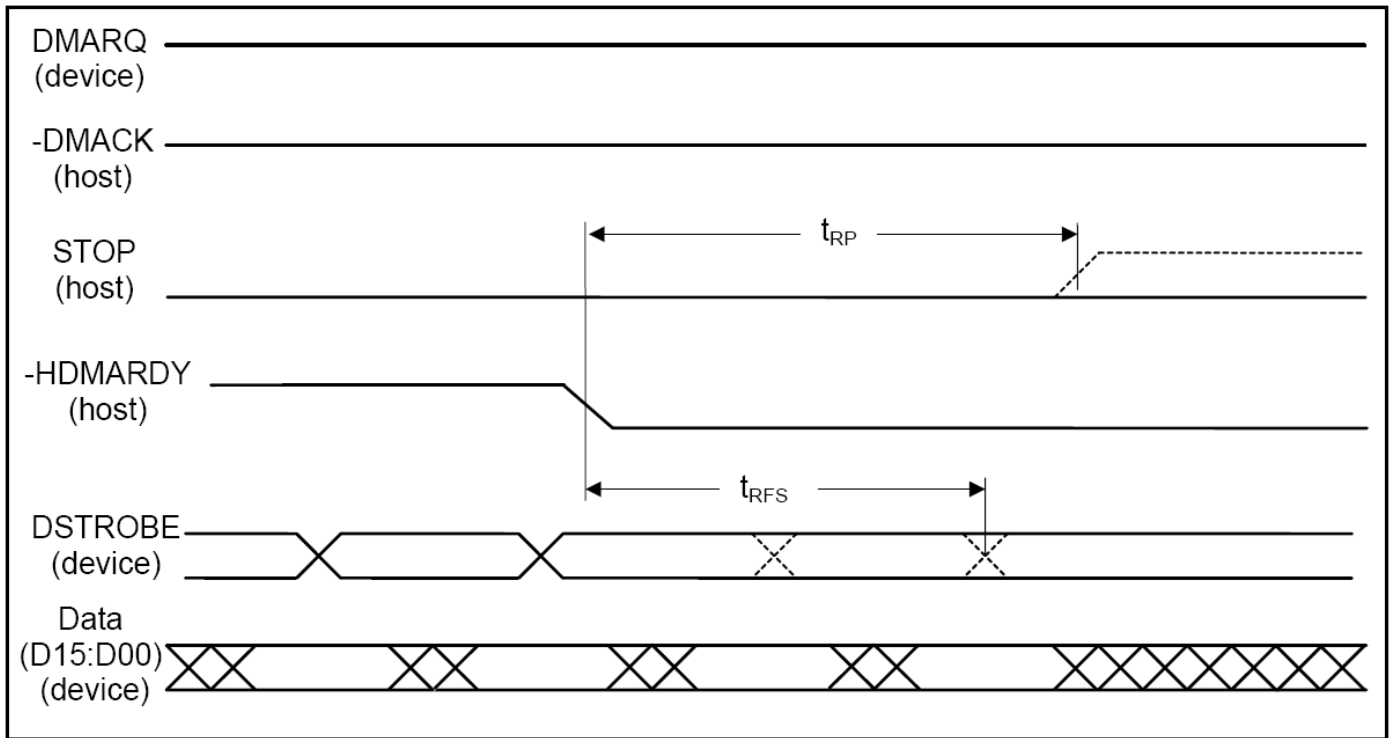
**Figure 15: Sustained Ultra DMA Data-In Burst**

4.11.4 Host Pausing an Ultra DMA Data-In Burst

The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in Figure 16: Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall pause an Ultra DMA burst by negating -HDMARDY.
- c) The device shall stop generating DSTROBE edges within  $t_{RFS}$  of the host negating -HDMARDY.
- d) If the host negates -HDMARDY within  $t_{SR}$  after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates -HDMARDY greater than  $t_{SR}$  after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and  $t_{RFS}$  timing for the device.
- e) The host shall resume an Ultra DMA burst by asserting -HDMARDY.



Notes:

- 1) The host may assert STOP to request termination of the Ultra DMA burst no sooner than  $t_{RP}$  after -HDMARDY is negated.
- 2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

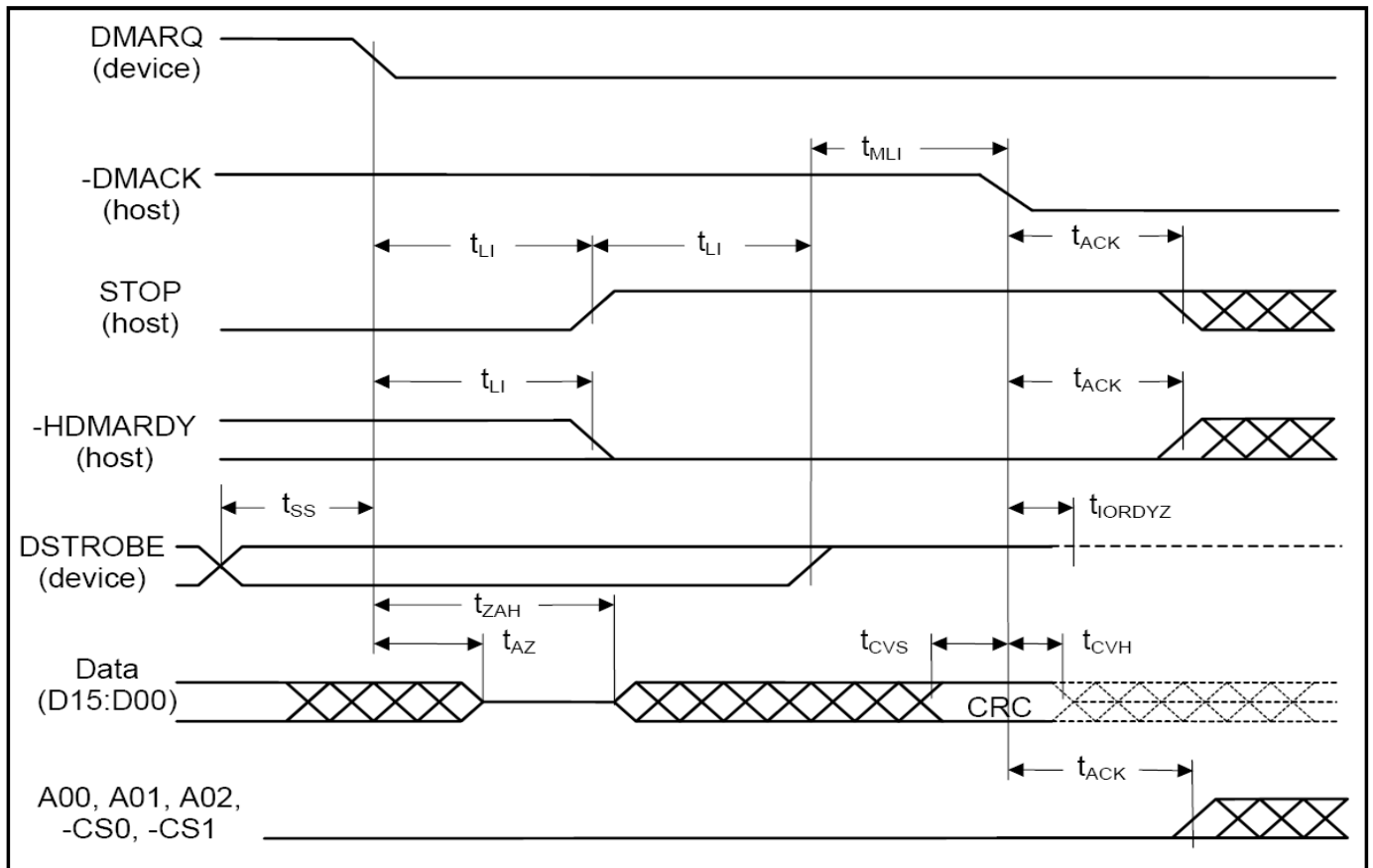
Figure 16: Ultra DMA Data-In Burst Host Pause Timing

4.11.5 Device Terminating an Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 17: Ultra DMA Data-In Burst Device Termination Timing. The timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.
- c) NOTE - The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate -HDMARDY and wait  $t_{RP}$  before asserting STOP.
- d) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

**Figure 17: Ultra DMA Data-In Burst Device Termination Timing**

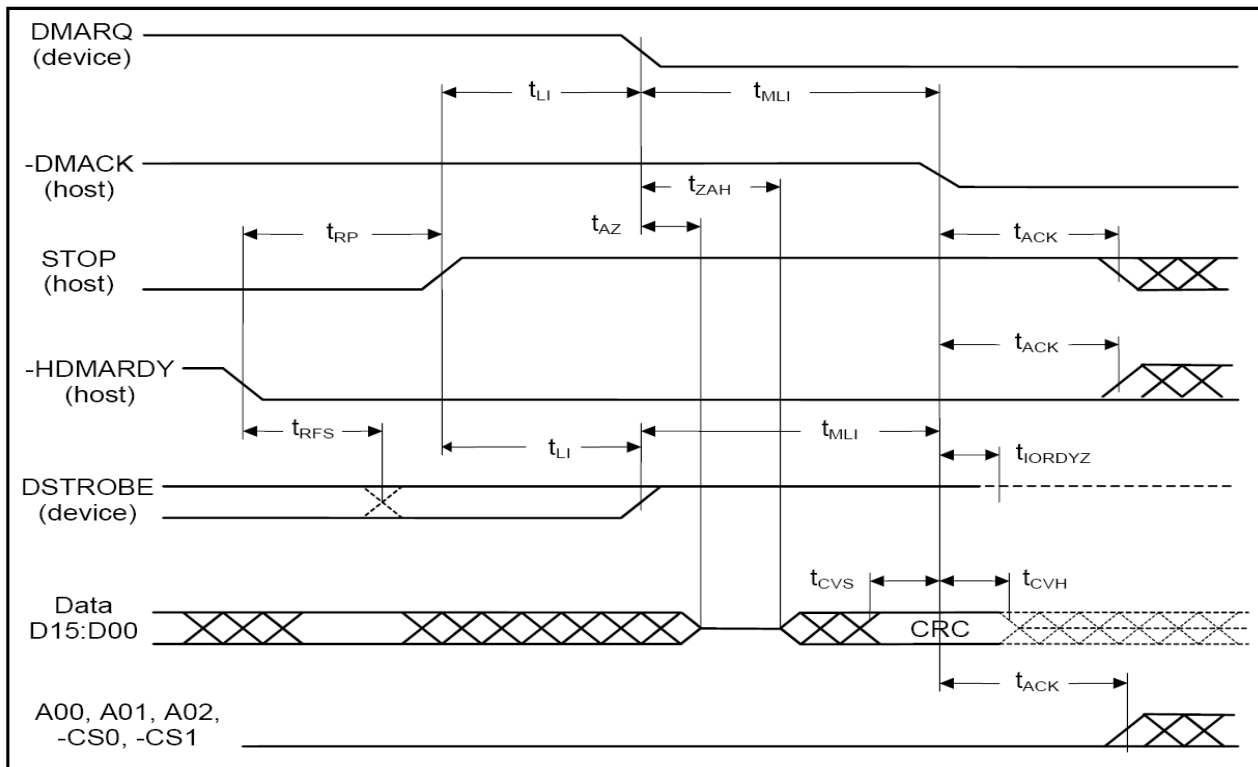
#### 4.11.6 Host Terminating an Ultra DMA Data-In Burst

The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 18: Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall initiate Ultra DMA burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA burst is terminated.
- c) The device shall stop generating DSTROBE edges within  $t_{RFS}$  of the host negating -HDMARDY.

- d) If the host negates -HDMARDY within  $t_{SR}$  after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY greater than  $t_{SR}$  after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and  $t_{RFS}$  timing for the device.
- e) The host shall assert STOP no sooner than  $t_{RP}$  after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- f) The device shall negate DMARQ within  $t_{LI}$  after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- g) If DSTROBE is negated, the device shall assert DSTROBE within  $t_{LI}$  after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- h) The device shall release D[15:00] no later than  $t_{AZ}$  after negating DMARQ.
- i) The host shall drive DD D[15:00] no sooner than  $t_{ZAH}$  after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation.
- j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00].
- k) The host shall negate -DMACK no sooner than  $t_{MLI}$  after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated -HDMARDY, and no sooner than  $t_{DVS}$  after the host places the result of its CRC calculation on D[15:00].
- l) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
- m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred.
- n) The device shall release DSTROBE within  $t_{IORDYZ}$  after the host negates -DMACK.
- o) The host shall neither negate STOP nor assert -HDMARDY until at least  $t_{ACK}$  after the host has negated -DMACK.
- p) The host shall not assert -IORD, -CS0, -CS1, DA2, DA1, or DA0 until at least  $t_{ACK}$  after negating DMACK



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated..

**Figure 18: Ultra DMA Data-In Burst Host Termination Timing**

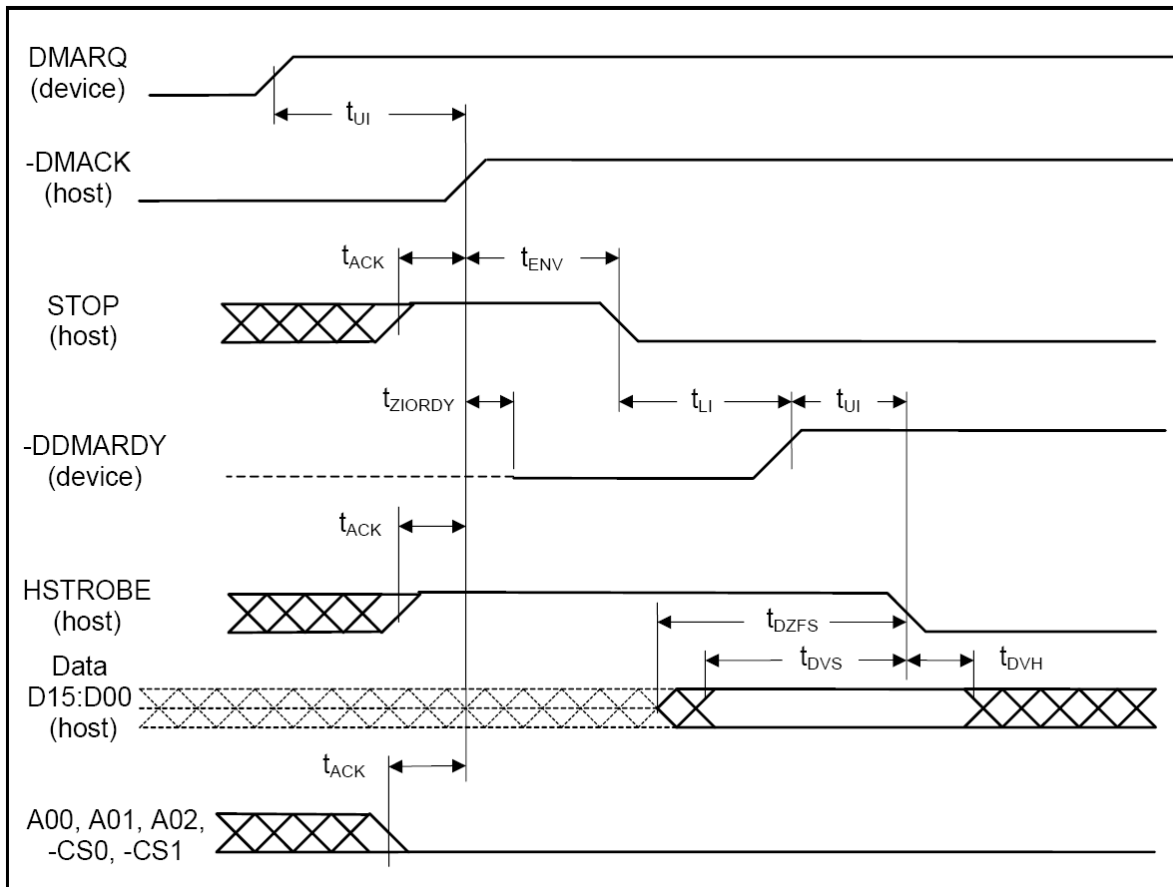
4.11.7 Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 19: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.
- b) The device shall assert DMARQ to initiate an Ultra DMA burst.
- c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
- d) The host shall assert HSTROBE.
- e) The host shall negate -CS0, -CS1, DA2, DA1, and DA0. The host shall keep -CS0, -CS1, DA2, DA1, and DA0 negated until after negating -DMACK at the end of the burst.
- f) Steps (c), (d), and (e) shall have occurred at least  $t_{ACK}$  before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.
- g) The device may negate -DDMARDY  $t_{ZIORDY}$  after the host has asserted -DMACK. Once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.
- h) The host shall negate STOP within  $t_{ENV}$  after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.

- i) The device shall assert -DDMARDY within  $t_{LI}$  after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.
- j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA burst initiation.
- k) To transfer the first word of data: the host shall negate HSTROBE no sooner than  $t_{UI}$  after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than  $t_{DVS}$  after the driving the first word of data onto D [15:00].



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

**Figure 19: Ultra DMA Data-Out Burst Initiation Timing**

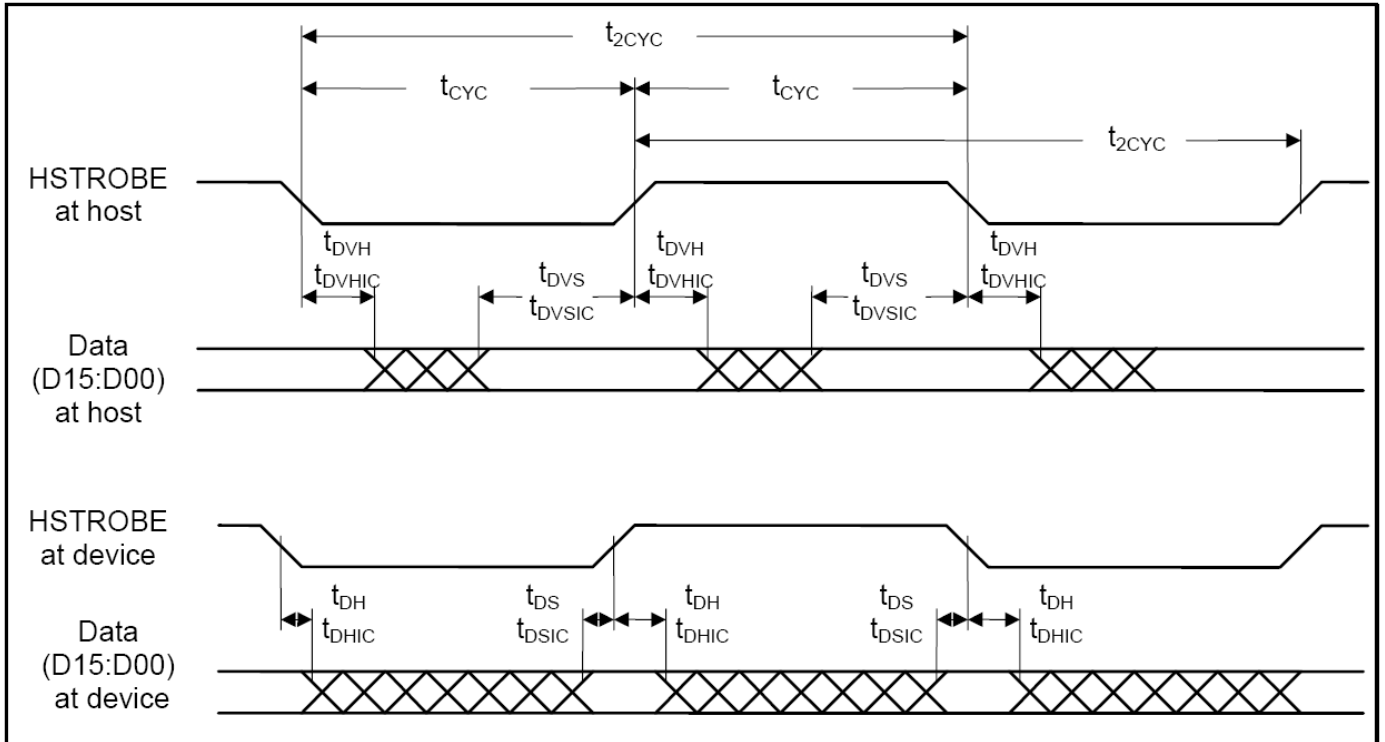
#### 4.11.8 Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 20: Sustained Ultra DMA Data-Out Burst Timing. The associated timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall drive a data word onto D [15:00].
- b) The host shall generate an HSTROBE edge to latch the new word no sooner than  $t_{DVS}$  after changing the state of D [15:00]. The host shall generate an HSTROBE edge no more frequently than  $t_{CYC}$  for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than  $2t_{CYC}$  for the selected Ultra DMA mode.

- c) The host shall not change the state of D[15:00] until at least  $t_{DVH}$  after generating an HSTROBE edge to latch the data.
- d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.



Note: Data (D15:D00) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

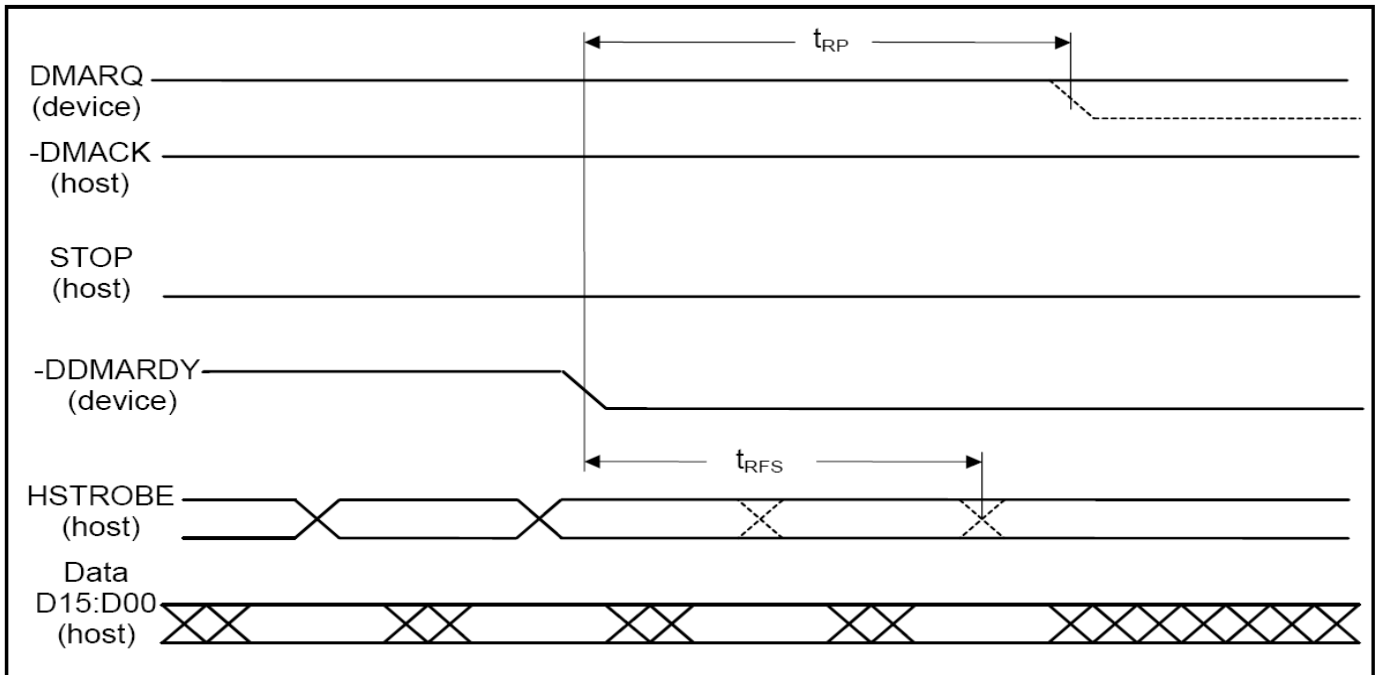
**Figure 20: Sustained Ultra DMA Data-Out Burst Timing**

4.11.9 Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in Figure 21: Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall pause an Ultra DMA burst by negating -DDMARDY.
- c) The host shall stop generating HSTROBE edges within  $t_{RFS}$  of the device negating -DDMARDY.
- d) If the device negates -DDMARDY within  $t_{SR}$  after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than  $t_{SR}$  after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and  $t_{RFS}$  timing for the host.
- e) The device shall resume an Ultra DMA burst by asserting -DDMARDY.



Notes: 1) The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than  $t_{RP}$  after -DDMARDY is negated.  
 2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

**Figure 21: Ultra DMA Data-Out Burst Device Pause Timing**

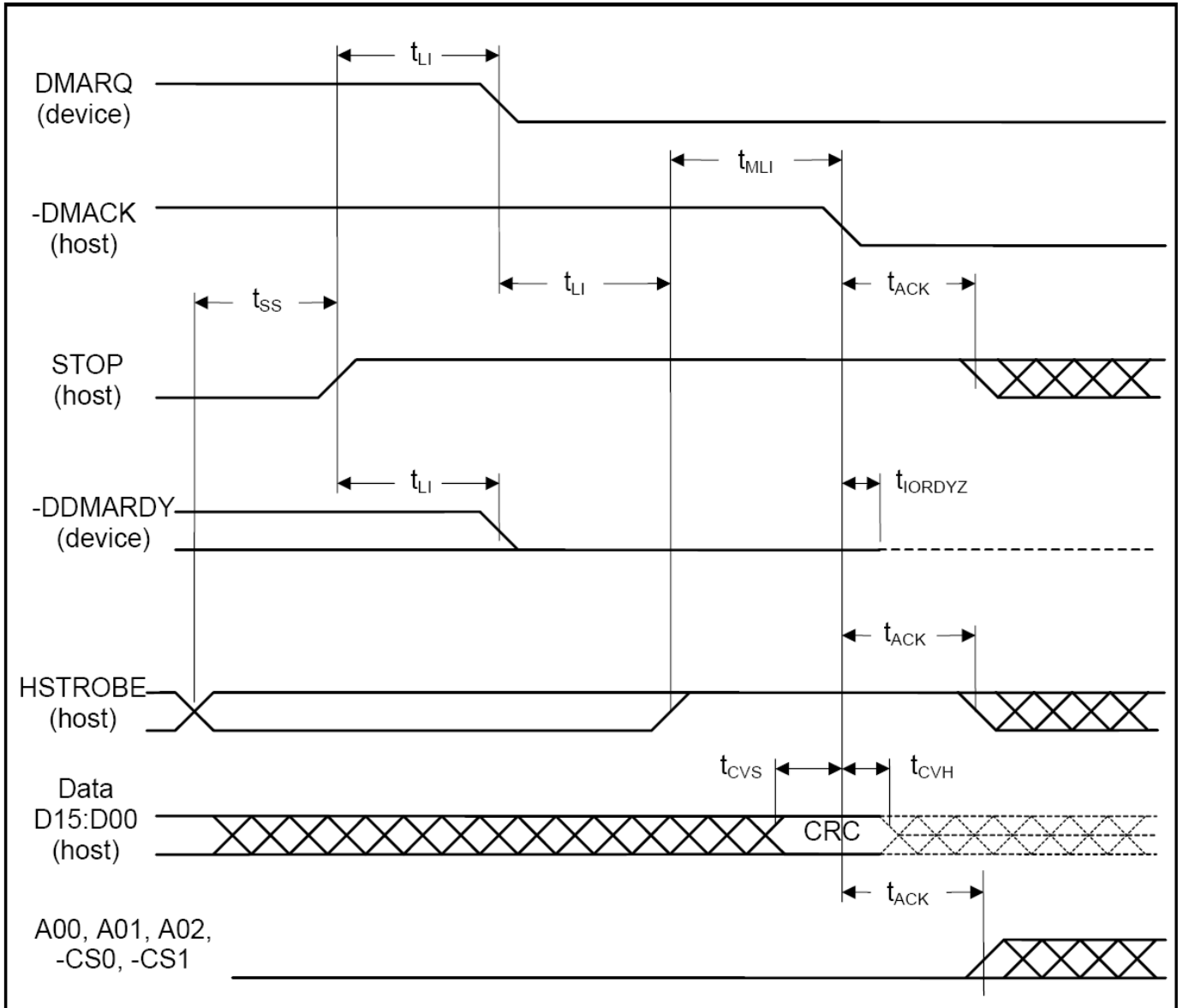
4.11.10 Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in Figure 22: Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall initiate Ultra DMA burst termination by negating -DDMARDY.
- c) The host shall stop generating an HSTROBE edges within  $t_{RFS}$  of the device negating -DDMARDY.
- d) If the device negates -DDMARDY within  $t_{SR}$  after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than  $t_{SR}$  after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and  $t_{RFS}$  timing for the host.
- e) The device shall negate DMARQ no sooner than  $t_{RP}$  after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- f) The host shall assert STOP within  $t_{LI}$  after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- g) If HSTROBE is negated, the host shall assert HSTROBE within  $t_{LI}$  after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- h) The host shall place the result of its CRC calculation on D[15:00]

- i) The host shall negate -DMACK no sooner than  $t_{MLI}$  after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than  $t_{DVS}$  after placing the result of its CRC calculation on D[15:00].
- j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
- k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a mis-compare error occurs during one or more Ultra DMA bursts for any one command,



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

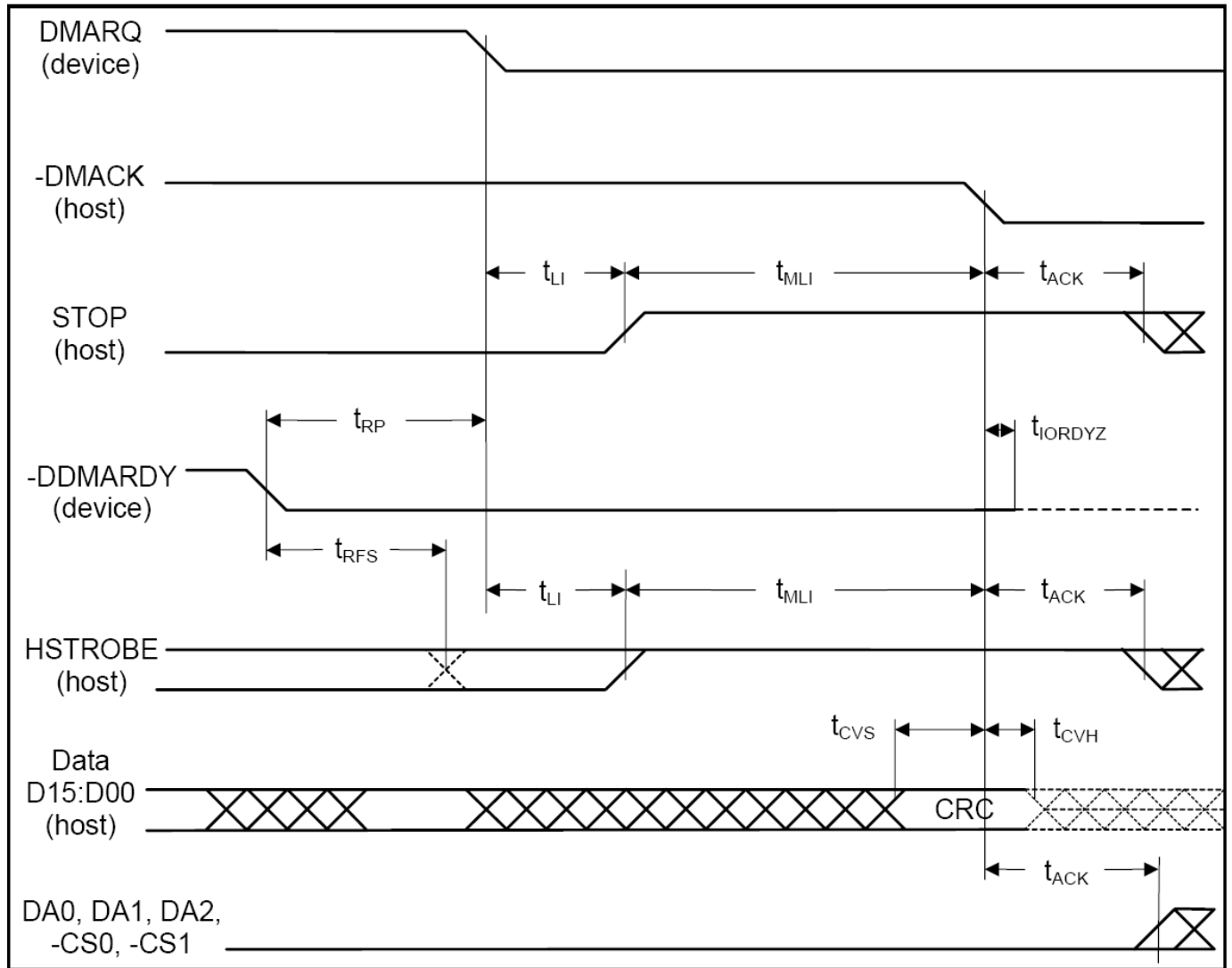
Figure 22: Ultra DMA Data-Out Burst Device Termination Timing

4.11.11 Host Terminating an Ultra DMA Data-Out Burst

Termination of an Ultra DMA Data-Out burst by the host is shown in Figure 23: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Table 15: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Table 16: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.
- b) The host shall assert STOP no sooner than  $t_{SS}$  after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- c) The device shall negate DMARQ within  $t_{LI}$  after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- d) The device shall negate -DDMARDY within  $t_{LI}$  after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA burst termination is complete.
- e) If HSTROBE is negated, the host shall assert HSTROBE within  $t_{LI}$  after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- f) The host shall place the result of its CRC calculation on D[15:00].
- g) The host shall negate -DMACK no sooner than  $t_{MLI}$  after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than  $t_{DVS}$  after placing the result of its CRC calculation on D[15:00].
- h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
- i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a mis-compare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.
- j) The device shall release -DDMARDY within  $t_{IORDYZ}$  after the host has negated -DMACK.
- k) The host shall neither negate STOP nor negate HSTROBE until at least  $t_{ACK}$  after negating -DMACK.
- l) The host shall not assert -IOWR, -CS0, -CS1, DA2, DA1, or DA0 until at least  $t_{ACK}$  after negating -DMACK.



Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

**Figure 23: Ultra DMA Data-Out Burst Host Termination Timing**

## 4.12 Card Configuration

### 4.12.1 Attribute Memory Function

Attribute memory is a space where CompactFlash Storage Card. identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the card configuration registers is 200h.

For the Attribute Memory Read function, signals -REG and -OE shall be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 19: Attribute Memory Function below for signal states and bus validity for the Attribute Memory function.

**Table 19: Attribute Memory Function**

Function Mode	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration CompactFlash Storage (8 bits)	L	H	L	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration CompactFlash Storage (8 bits)	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration CompactFlash Storage (16 bits)	L	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration CompactFlash Storage (16 bits)	L	L	L	L	H	X	H	L	Don't Care	Even Byte

Note: The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.

### 4.12.2 I/O Transfer Function

The I/O transfer to or from the CompactFlash Storage can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Storage. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Storage, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds.

The CompactFlash Storage may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

**Table 20: PCMCIA Mode I/O Function**

Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

4.12.3 Common Memory Transfer Function

The Common Memory transfer to or from the CompactFlash Storage can be either 8 or 16 bits. The CompactFlash Storage Card permit both 8 and 16 bit accesses to all of its Common Memory addresses.

The CompactFlash Storage Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

**Table 21: Common Memory Function**

Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

#### 4.12.4 True IDE Mode I/O Transfer Function

The CompactFlash Storage Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash Storage Cards may support the following optional detection methods:

1. The card is permitted to monitor the -OE (-ATA SEL) signal at any time(s) and switch to PCMCIA mode upon detecting a high level on the pin.
2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-) RESET pin.
3. The card is permitted to monitor the -OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time.

Host implementers should not rely on any of these optional detection methods in their designs. In the True IDE Mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. CompactFlash Storage Cards permit 8 bit PIO mode data accesses if the user issues a Set Feature Command to put the CompactFlash Storage Card in 8 bit Mode.

Note: Removing and reinserting the CompactFlash Storage Card while the host computer's power is on will reconfigure the CompactFlash Storage Card to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash Storage Card in True IDE Mode, the 50-pin socket is power cycled with the CompactFlash Storage Card inserted and -OE (output enable) asserted.

**Table 22: True IDE mode I/O Function**

Function Codes	-CS1	-CS0	A0-A2	-DMACK	-IORD	-IOWR	D15-D8	D7-D0
Invalid Modes	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined in	Undefined in
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined in	Undefined in
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte in	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte in	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 2		Odd-Byte in	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 3		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address <sup>1</sup>	L	H	7h	H	L	H	High Z	Data Out

Notes:

- 1) Implemented for backward compatibility. Bit D7 of the register shall remain High Z to prevent conflict with any floppy disk controller at the same address. The host software should not rely on the contents of this register.
- 2) In Ultra DMA Data Register Write mode the signals –IORD, –IOWR and IORDY are redefined and used as follows: –IORD as HSTROBE, –IOWR as STOP and IORDY as –DDMARDY. Data transfers with each edge of HSTROBE.
- 3) In Ultra DMA Data Register Read mode the signals –IORD, –IOWR and IORDY are redefined and used as follows: –IORD as –HDMARDY H, –IOWR as STOP and IORDY as DSTROBE. Data transfers with each edge of DSTROBE.

5. CF-ATA Command Set list

Table 23: CF-ATA Command Set List

Command	Command code	Used parameter					
		FR	SC	SN	CY	DH	LBA
CFA ERASE SECTOR(S)	C0H	-	Y	Y	Y	Y	Y
CFA REQUEST EXTENDED ERROR CODE	03H	-	-	-	-	D	-
CFA TRANSLATE SECTOR	87H	-	-	Y	Y	Y	Y
CFA WRITE MULTIPLE WITHOUT ERASE	CDH	-	Y	Y	Y	Y	Y
CFA WRITE SECTOR(S) WITHOUT REASE	38H	-	Y	Y	Y	Y	Y
Check power mode	E5H or 98H	-	-	-	-	D	-
Execute drive diagnostic	90H	-	-	-	-	-	-
Flush cache	E7H						
Format track	50H	-	Y	Y	Y	Y	Y
Identify Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle immediate	E1h or 95h	-	-	-	-	D	-
Initialize drive parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read buffer	E4H	-	-	-	-	D	-
Read DMA	C8h,C9h	-	Y	Y	Y	Y	Y
Read long sector	22H or 23H	-	-	Y	Y	Y	Y
Read multiple	C4H	-	Y	Y	Y	Y	Y
Read sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read verify sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
Recalibrate	1Xh	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set features	EFH	Y	-	-	-	D	-
Set multiple mode	C6H	-	Y	-	-	D	-
Set sleep mode	E6h or 99h	-	-	-	-	D	-
Stand by	E2h or 96h	-	-	-	-	D	-
Stand by immediate	E0h or 94h	-	-	-	-	D	-
Write buffer	E8H	-	-	-	-	D	-
Write DMA	CAH,CBH	-	Y	Y	Y	Y	Y
Write long sector	32h or 33h	-	-	Y	Y	Y	Y
Write multiple	C5H	-	Y	Y	Y	Y	Y
Write sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write verify	3CH	-	Y	Y	Y	Y	Y
Wear level	F5H	-	-	-	-	D	-

Definitions:

- FR = Features Register
- SC = Sector Count Register
- SN = Sector Number Register
- CY = Cylinder Registers
- DH = Card/Drive/Head Register
- LBA = Logical Block Address Mode Supported (see command descriptions for use).
- Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Storage Card and head parameters are used; D - only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command descriptions for use).

6. Ordering Information

Table 24: CompactFlash Storage Card Ordering Information

P/N	Capacity (Max)
AC73-1280 1R04XX*2	8GB

\*1 : 1280:128MB, 2560:256MB, 5120:512MB, 1030:1GB, 2030:2GB, 4030:4GB, 8030:8GB

\*2 : 1~8 (single mode): capacity: 128MB~2GB, Data Transfer: Read: up to 10MB/sec; Write: up to 5MB/sec  
 A ~ H (dual mode): capacity: 256MB~8GB, Data Transfer: Read: up to 20MB/sec; Write: up to 10MB/sec

7. Contact Information

CoreSolid Storage Corporation, a TDK-PQI storage business company, specializes in the design and marketing of SSD, DOM, and Industry CF products.

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