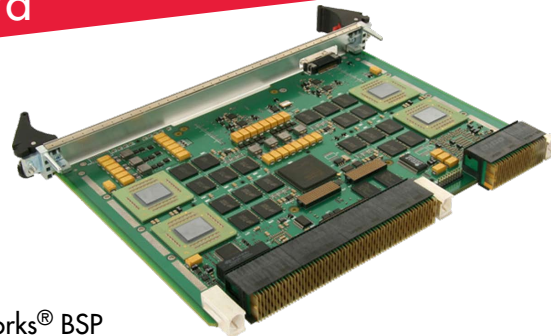




Data Sheet

# CHAMP-AV6

Quad/Octal Freescale Power Architecture™ MPC8640/8641  
VPX Card



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### Features

- ◆ Four Freescale Power Architecture™ MPC8640/8641 dual-core CPUs at 1.0GHz
- ◆ Up to eight processor cores
- ◆ On-board Serial RapidIO® (SRIO) interconnect
- ◆ Four SRIO ports to the VITA 46 core fabric
- ◆ Option for PCI Express® (PCIe) port to the VITA 46 core fabric
- ◆ Up to 1GB DDR2 SDRAM with ECC per processor
- ◆ Up to 256MB Flash with write protection
- ◆ Protected backup Flash
- ◆ 128KB nvSRAM
- ◆ Gigabit Ethernet (GbE) per processor
- ◆ On-board GbE switch
- ◆ One XMC site with x8 PCIe interface
- ◆ Additional x8 PCIe interface to the backplane
- ◆ Four EIA-232 serial ports
- ◆ Two EIA-422 serial ports
- ◆ Multi-board synchronous clock
- ◆ Temperature sensors
- ◆ 16 discrete LVTTL I/O signals

- ◆ VxWorks® BSP
- ◆ Continuum Insights multi-processor development tools
- ◆ Continuum Vector™ DSP Library
- ◆ Mechanical formats
  - VITA 48.1 type 2 air-cooled 1" pitch
  - VITA 48.2 type 2 conduction-cooled 1" pitch
  - VITA 48.2 type 1 conduction-cooled 1" pitch (covered, 2-level maintenance LRM)

### Overview

The CHAMP-AV6 quad Power Architecture board pairs Freescale's latest AltiVec™-enabled processor with the serial switched fabric capabilities native to the new COTS standard, VITA 46. The VITA 46 standard was collaboratively developed by COTS industry leaders and system integrators to marry high-speed serial interconnect with a form factor and feature set specifically suited to a variety of embedded computing applications.

Multi-processor systems based on the CHAMP-AV6 will benefit from the 10GB/s full duplex bandwidth provided by four SRIO ports, approximately 10x faster than the best VME/StarFabric implementation.



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## VPX-REDI Module Format

The Versatile Performance Switching (VPX) module format, governed by the VITA 46 specification and the associated VITA 48 Ruggedized Enhanced Design Implementation (REDI) was established to address the fundamental requirement to provide open-architecture modules that incorporate the high-speed serial interconnect technology that is becoming pervasive in high performance computing. The VPX standard was developed by the leading providers of COTS modules to address the major issue of high-speed serial interconnect, as well as incorporating numerous improvements learned after years of integrating VME and CompactPCI (cPCI) modules. The VPX standard, in short provides:

- ◆ 3U and 6U Eurocard form factors preserve chassis mechanical designs
- ◆ Support four x4 serial interfaces as the primary fabric
- ◆ Support 128 differential pairs for modern high-speed interfaces such as DVI, SATA, SFPDP, SAS and custom sensor interfaces
- ◆ Support for higher power modules and improved cooling
- ◆ Improved logistics with two-level maintenance and keying

The VPX module format provides many benefits to integrators of high performance multi-processor systems for radar, electro-optical and signal intelligence applications. In particular, the 10GB/s off-card bandwidth using SRIO technology and additional 7.75GB/s of additional user I/O bandwidth will unleash the next generation multi-core processors and FPGAs.

## Processor Nodes

The CHAMP-AV6 architecture incorporates four Freescale Power Architecture MPC8641/8641D processors. The MPC8641 provides in a single package one or two e600 cores, dual DDR2 memory controllers with ECC, a SRIO interface, a PCIe interface, GbE controllers and serial I/O controllers.

The e600 core and AltiVec units of the MPC8641 processor are based on the proven internals of the MPC7448 processor, offering a large 1MB internal L2 cache. Existing C, assembly and AltiVec assembly code will run on the MPC8641 without change. At 1GHz, the dual-core equipped CHAMP-AV6 provides 64 GFLOPs of computing performance.

## On-card Fabric

The CHAMP-AV6 utilizes SRIO interconnect to provide high-speed processor to processor communications. Using the native SRIO port of the MPC8641, each processor has a 4-lane interface capable of simultaneous 1.25GB/s transmit and receive for a total of 2.5GB/s of communications bandwidth. A Tundra® TSI578 8-port SRIO switch provides local switching as well as routing four SRIO ports to the VPX core fabric connectors. Multiple CHAMP-AV6 cards may be inter-connected using the SRIO core fabric interface. The four SRIO ports support a maximum bandwidth of 5GB/s transmit and receive for a total of 10GB/s. The on-board switch function facilitates building systems of multiple cards without an external switch card.

Figure 1, the CHAMP-AV6 Block Diagram shows the architecture of the card and the I/O interfaces provided.

The CHAMP-AV6 may be optionally factory configured to provide one PCIe interface on the core fabric connector. The PCIe interface may be used to connect to PCIe-based XMC/PMC carrier cards or other PCIe/ASI-based processor cards.

## Additional PCIe Interface

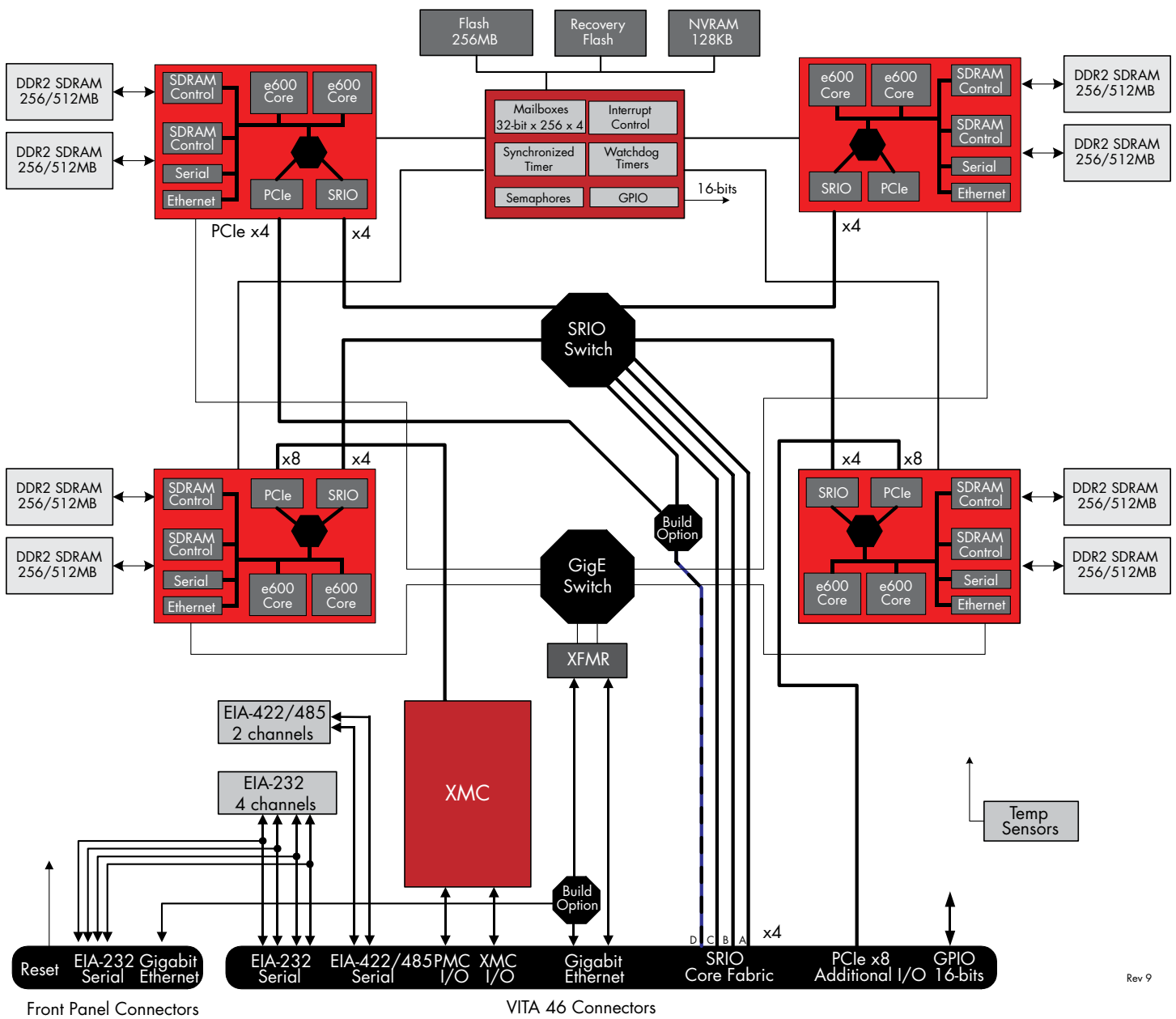
For additional connectivity with sensor I/O cards the CHAMP-AV6 provides an additional 8-lane PCIe interface to a user I/O backplane connector. The PCIe interface is directly connected to one of the processor nodes. Demonstrating the benefit of the VPX module format, this interface provides an additional I/O bandwidth of 2GB/s transmit and receive (4GB/s total) in addition to the 10GB/s provided by the core SRIO fabric.

## Double Data Rate SDRAM

Each processor node on the CHAMP-AV6 supports 256MB to 1GB of DDR2 SDRAM with support for 2GB when the next generation of devices become available. The CHAMP-AV6 supports the dual memory controller feature of the MPC8641 processor, providing a peak memory bandwidth of 8.0GB/s. The memory is protected with Error Checking and Correcting (ECC) circuitry that can detect and correct all single-bit errors and detect all double-bit errors. The high memory bandwidth will support demanding streaming data applications with simultaneous occurrence of dataflow from the processors and SRIO interfaces.



Figure 1: CHAMP-AV6 Block Diagram



Rev 9



## Flash Memory

The CHAMP-AV6 is equipped with 256MB of Flash memory. The 32-bit wide interface supports peak transfer rates of 120MB/s to minimize boot and program loading times. For absolute security against inadvertent Flash programming or corruption, a hardware jumper is provided to disable write access to the Flash.

## Protected Access Boot Site (PABS)

The CHAMP-AV6 has a secondary Flash subsystem, PABS, which provides a backup boot facility. PABS is typically used in two scenarios. The first is recovery from corruption of the primary Flash memory. The CHAMP-AV6 can be made to boot from PABS by asserting a control signal on the backplane or via an on-board jumper. Once the PABS resident firmware is booted the main Flash can be programmed to re-instate the standard firmware. The second scenario is the support of de-classification requirements. PABS firmware provides de-classification functions that will scrub the contents of main Flash. Since the PABS Flash is hardware write-protected, the user is ensured that no classified data can be written inadvertently to PABS.

## nvSRAM

A 128KB auto-store nvSRAM provides nonvolatile storage of mission state data that must not be lost when power is removed. During normal operation, application software reads and writes the nvSRAM just like standard SRAM. Upon power loss, the nvSRAM automatically transfers its contents to on-chip EEPROM. Upon power-up, the EEPROM contents are transferred back to the SRAM, where the application can utilize the stored data to continue normal operation. The number of recall cycles is unlimited: the maximum number of store cycles is 1,000,000 and the data retention period is 100 years. For security against inadvertent writes to nvSRAM, a hardware write-protection feature is provided.

## Gigabit Ethernet With On-board Switching

Each processor node of the CHAMP-AV6 is equipped with a GbE interface, implemented via the Ethernet controller within the MPC8641 processor. The Ethernet controller includes features designed to minimize processor loading due to Ethernet traffic including dedicated DMA engines, support for jumbo packets up to 9KB, checksum calculations and hardware support for IPv6.

The GbE interface of each processor node is routed to an on-board Broadcom® 5388 8-port GbE switch. Two ports from the switch are routed to the backplane connector. The on-board switch permits network access to all the processors via either or both of the external GbE ports. The CHAMP-AV6 can be used in high performance networking environments in conjunction with an external Ethernet switch, or if the network traffic is less demanding, multiple CHAMP-AV6 cards may be daisy-chained together relying on the on-board switch to route packets to the adjacent cards as needed.

Air-cooled versions of the CHAMP-AV6 route one Ethernet port to a front panel connector as standard and optionally both Ethernet ports are routed to the backplane connectors.

## XMC Site

The VITA 42 standard and subsidiary specifications define the XMC mezzanine module format which adds high-speed data interfaces and I/O capability to the PMC standard. Together these improvements allow for the next generation of mezzanine modules with improved throughput to the host processor and dramatically increased I/O bandwidth. The CHAMP-AV6 is equipped with one XMC mezzanine site supporting a PCIe interface. The XMC site is directly connected to the PCIe interface of Processor B. The card supports an 8-lane (x8) interface capable of 2GB/s simultaneous in both transmit and receive directions, for a total of 4GB/s.

The XMC site provides both traditional PMC I/O, single-ended XMC I/O and high-speed differential XMC I/O. 64-bits of I/O are routed from the Pn4 connector to the CHAMP-AV6 backplane connector. 38-bits of single-ended user I/O and 20-pairs of high-speed differential I/O are routed via the XMC's high-speed capable Pn6 connector to the backplane, supporting signaling rates to the XMC of 3.125GB/s when used in differential pairs.

The conduction-cooled versions of the CHAMP-AV6 adhere to the IEEE 1386-2001 and ANSI/VITA 20 standard for conduction-cooled PMCs. The CHAMP-AV6 thermal frame provides the best possible thermal interface for mezzanine modules by supporting the primary and secondary thermal interfaces as defined by ANSI/VITA-20. To support high power XMC modules, the CHAMP-AV6 thermal frame supports a mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed XMC modules



can significantly lower the temperature rise between the CHAMP-AV6 card edge and the XMC components. The mid-plane thermal shunt does not impinge on the IEEE 1386-2001 specified component height.

### Utility Features Mailbox, Semaphores & Timers

The CHAMP-AV6 features a number of utility features to facilitate multi-processor software applications.

Each processor (core) has a mailbox interrupt mechanism whereby a processor can interrupt another processor and deliver a 32-bit value. Each processor has a 32-bit, 256-deep FIFO. Any processor can write to the FIFO of any other processor. An entry in the FIFO causes an interrupt to the associated processor, if enabled. The software can use the 32-bit value to include a message with the interrupt. The combination of a separate data path and the inclusion of a 32-bit message can significantly reduce the latency of using interrupts to send messages between processors.

The board provides sixteen hardware semaphore registers which are typically used to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques and avoids the use of shared memory to access the semaphores.

In addition to the timer resources within the MPC8641, the CHAMP-AV6 provides four general purpose 32-bit timers which may optionally cause an interrupt to any processor upon rollover and be preset with an interval value.

### Avionics Style Watchdog Timer

The CHAMP-AV6 provides a watchdog timer for each of the processor cores (up to eight). Each watchdog timer is a pre-settable down-counter with a resolution of 1  $\mu$ sec. Time-out periods from 1 ms to 32 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts.

The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between

writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. In other words, writing to the watchdog register too soon or too late causes an exception event.

### Multi-board Synchronous Clock

The CHAMP-AV6 includes a special purpose counter which may be synchronized with corresponding counters on other boards in the same system. This common time base allows a developer to time-stamp messages and/or data buffers, with the knowledge that the local time is maintained at the same value by all the boards in the system. The counter can be set to roll-over to a pre-load value and interrupt on roll-over. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors.

### Serial Ports

The CHAMP-AV6 provides four EIA-232 serial ports and two EIA-422 serial ports.

Each processor has one EIA-232 serial port, utilizing the MPC8641 DUART. The EIA-232 serial ports support asynchronous communications with one transmit and one receive signal. All four ports are connected to both a front panel connector and the backplane connector. One serial port supports the use of the DTR signal to automatically detect the connection of a data terminal and can be used to control the boot-up sequence of the card if desired. The EIA-232 ports support operation up to 115 Kbaud.

Two processors nodes (A and B) are provided with an EIA-422 differential serial port utilizing the MPC8641 DUART. The EIA-422 ports support asynchronous communications with one transmit and one receive pair each. The EIA-422 ports are connected to the backplane connectors.

### LVTTTL Discrete Digital I/O

The CHAMP-AV6 provides sixteen general purpose LVTTTL I/O lines which are accessible at the backplane connector. Each bit is individually programmable to be an input, output or I/O. All bits configured as an input may be used to trigger an interrupt which is further programmable to be



level or edge sensitive. Both levels and transition directions may be detected. The LVTTL I/O lines are terminated with an on-board pull-up resistor.

### Differential Discrete Digital I/O

The CHAMP-AV6 provides the capability to control discretely, the outputs of the two EIA-422 drivers which are normally associated with EIA-422 serial channels. In a similar fashion, there are registers that can read the state of the EIA-422 receivers, independent of the serial controller. In total there are two inputs and two outputs. The inputs may be configured to generate an interrupt. When configured as discrete differential I/O, the drivers and receivers used as general-purpose differential-mode control signals unrelated to serial I/O.

### Temperature Sensors

The CHAMP-AV6 provides temperature sensors to measure board and processor temperatures. Two sensors are located along each edge of the board, and one sensor per processor is provided. The sensors can be read by software, and they may be configured to generate an interrupt in case of an over temperature condition.

### Indicator LEDs

The CHAMP-AV6 provides eight user-controllable LEDs. These are visible on the front panel of both air-cooled and conduction-cooled versions. There is an additional red LED on the front panel of both versions used to indicate a failure determined by the on-board diagnostic firmware.



### Continuum Software Architecture (CSA)

The CHAMP-AV6 is supported by a suite of firmware, RTOS board support packages (BSP), communication libraries and signal processing libraries. The Continuum Software Architecture is Curtiss-Wright Controls' suite of firmware and BSP APIs that is common to Single Board Computers (VME, cPCI and VPX) and multi-processor boards. Developers of mixed systems will find a common set of features and software interfaces for all future processing products from Curtiss-Wright Controls. The Continuum Software Architecture is comprised of:

**Continuum Firmware Monitor** - provides a command line interface over serial port or Ethernet to allow a user to perform a variety of system integration activities with the card. The monitor provides debug and display commands, diagnostic results display and exerciser controls, non-volatile memory programming and declassification and programming of parameters used to control boot-up and diagnostics.

**Built-in-Test (BIT)** - a library of diagnostic routines to support Power-up BIT (PBIT), and Initiated BIT (IBIT) designed to provide 95% fault coverage.

### Operating System Software

The CHAMP-AV6 is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported on the CHAMP-AV6:

- ◆ VxWorks 6.x, Workbench 2.x from Wind River. (Part number DSW-460-000-CD)

### Continuum Insights

The Continuum Insights visualization and instrumentation tools are designed to ease and optimize the development of application software for multi-computer embedded systems. The Insights suite of tools is based on the Eclipse Development and Application Framework, and includes an Event Analysis Tool, a System Monitoring Tool and System Management Functions. See the Continuum Insights datasheet for detailed information.

The Event Analysis tool provides an extension to the Wind River System Viewer tool to provide a post run-time view of time-correlated events across multiple processors in a system. The Event Analysis tool greatly simplifies the process of testing, verifying and debugging complex multiprocessor software.

The System Monitoring tool provides a hierarchical, graphical representation of a system of VPX boards. Chassis, board and processor views present dozens of hardware and software information items with real-time updates of processing thread, utilization, task allocation and other status information such as board temperatures. The System Management tool automates the startup of a



multi-computer with user libraries and executables. The tool manages the contents of all Flash devices in a system, individually or in defined groups. Users can work with multiple targets simultaneously using a facility to group telnet sessions to a single console with color coding and interleaving for easy delineation.

### Continuum IPC Library

The Continuum Inter-processor Library (IPC) is a library of functions designed to enable high performance, low-latency message passing. IPC allows processors to communicate task-to-task, on the same card over local interconnect or between boards over a system level interconnect. IPC supports several transport mechanisms including PCI, StarFabric and SRIO. Applications developed on previous generation VME-based systems will port to the CHAMP-AV6 with no changes related to the IPC layer.

IPC provides low-overhead block data transfers, segmented block data transfers and signaling between processors to assist in high bandwidth data movement. See the IPC Library datasheet for more details.

### Continuum Vector™ Library

The CHAMP-AV6 derives its floating-point performance from the Power Architecture AltiVec unit. Programming the AltiVec is complex. For customers who prefer to focus on their algorithms, Curtiss-Wright Controls offers the Continuum Vector DSP function library. Continuum Vector provides over 200 functions, providing the foundation for most signal processing applications. Continuum Vector provides the user with a choice of APIs with support for Vector Signal Image Processing Library (VSIPL, Core Lite) standard and the popular API established by Floating Point Systems Inc. See the Continuum Vector datasheet for detailed information.

### Options

The following configuration options are planned:

- ◆ Single and dual-core processors
- ◆ DDR2 SDRAM sizes of 512MB and 1GB per processor
- ◆ Four SRIO ports or three SRIO and one PCIe to the core fabric connector
- ◆ Air-cooled, conduction-cooled and two-level maintenance covered conduction-cooled

### Ordering Information

The CHAMP-AV6 is ordered with the following part numbers:

VPX6-460-UVWXY

- ◆ "U" denotes the cooling method
  - A = air-cooled
  - C = conduction-cooled
- ◆ "V" denotes the temperature range
  - 0 = 0°C - 50°C
  - 1 = -40°C - 71°C
  - 2 = -40°C - 85°C
- ◆ "W" denotes the mechanical format
  - 4 = 1" pitch
  - 5 = 1" pitch
  - 2-level maintenance support
- ◆ "X" denotes the backplane core fabric configuration
  - B = 4 SRIO ports
  - D = 3 SRIO ports
  - 1 PCIe port
- ◆ "YYY" identifies a specific configuration that typically describes processor speed, memory and other configurable options

A formal quote from Curtiss-Wright Controls or authorized representative will provide a complete part number and description of the configuration.



## Specifications

**Table 1: Champ-AV6 Power Requirements**

Power Requirements (without PMCs)	
3.3V Aux	20mA
5V	3.9A
12V	3.7A - 4.9A (single-core estimated MPC8640) 5.2A - 7.3A (dual-core estimated MPC8640)
-12V	Used only for XMC power

**Table 2: CHAMP-AV6 Dimensions & Weight**

Dimensions and Weight		
Option	Dimension	Weight
Air-cooled level 0	Per VITA 48 draft 1" pitch	960g (2.11lbs)
Air-cooled level 1	Per VITA 48 draft 1" pitch	1010g (2.2lbs)
Conduction-cooled	Per VITA 48 draft 1" pitch	1250g (2.75lbs)

Air-cooled cards available in temperature ranges 0 and 1.\*  
 Conduction-cooled cards available in temperature ranges 1 and 2.  
 Conduction cooled cards available in a covered, 2-level maintenance LRM configuration.  
 \* Refer to Urgidization Guidelines data sheet for more information.

**Table 3: CHAMP-AV6 Cooling Requirement**

Cooling Air Requirements		
Configuration	Temperature Range	Air-flow
Single-core	0° - 55°C	15 CFM
Single-core	-40° - 71°C	15 CFM
Dual-core	0° - 55°C	15 CFM
Dual-core	-40° - 71°C	24 CFM

Air-flow is specified for sea-level conditions. The temperature refers to the inlet temperature at the card. The CHAMP-AV6 requires cooling air to flow from bottom to top. The air-flow specifications are for worst case (highest power) conditions, without an XMC installed. Curtiss-Wright Controls can supply additional recommendations for specific power/temperature/altitude scenarios to support the design and testing of cooling subsystems.

## Warranty

This product has a one year warranty.

## Contact Information

To find your appropriate sales representative, please visit:

Website: [www.cwembedded.com/sales](http://www.cwembedded.com/sales)

Email: [sales@cwembedded.com](mailto:sales@cwembedded.com)

For technical support, please visit:

Website: [www.cwembedded.com/support1](http://www.cwembedded.com/support1)

Email: [support1@cwembedded.com](mailto:support1@cwembedded.com)

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