



Data Sheet

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# AD1500

## Dual 1.5GSPS Analog Input XMC/PMC

### Applications

- ♦ Electronic Counter Measures (ECM)
- ♦ Spectral Analysis
- ♦ RADAR

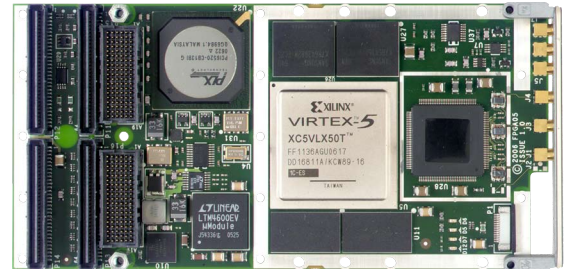
### Features

- ♦ 2x 1.5GSPS, 8-bit ADC
- ♦ Xilinx® Virtex®-5 SX95T FPGA (user programmable)
- ♦ Dual banks of QDR2 SRAM and DDR2 SDRAM memories
- ♦ Capable of multi-board synchronization
- ♦ XMC/PMC form factor
- ♦ Air- or conduction-cooled rugged versions
- ♦ Windows®, VxWorks® and Linux® support

### Benefits

- ♦ Combined acquisition and data processing
- ♦ Lower power solution
- ♦ Industry standard form factor
- ♦ PCI Express® (PCIe) provides high throughput to baseboard
- ♦ For use in deployed or commercial environments

### Overview



The AD1500 closely couples a high performance Xilinx Virtex-5 FPGA to a dual channel high-speed analog input front end providing both processing and up to 1.5GSPS acquisition (per channel) in a single XMC/PMC card. The combination of a user programmable FPGA, data I/O sub-systems and multiple banks of fast memory provides a powerful platform for acquiring and processing high-speed data in one board. In addition to processing digitized data, the Xilinx Virtex-5 SXT FPGA is used to control the analog to digital converter and provides the off-board interfaces to either PCI-X or the multi-GB/s serial I/O used for the XMC interface.

### Analog I/O & FPGA Processing in One

The AD1500 is a combined acquisition and FPGA based data processing module. The majority of the Virtex-5 FPGA resources are available for user programmable processing and are supported by SRAM and SDRAM memories. Some applications that are ideally suited for FPGA based processing include Digital Down Conversion (DDC), Fast Fourier Transforms (FFTs) and digital filters.

### 1.5GSPS Analog Input

Analog to digital conversion is performed by a National Semiconductor ADC08D1500 device, which is a dual channel 8-bit, 1.5GSPS ADC. The analog input stages are transformer AC coupled to the ADC via a balun. Using the ADC's built-in demultiplexer, digitized data is transferred to the FPGA using an interleaved 32-bit interface (2+2 samples in parallel).

Learn More

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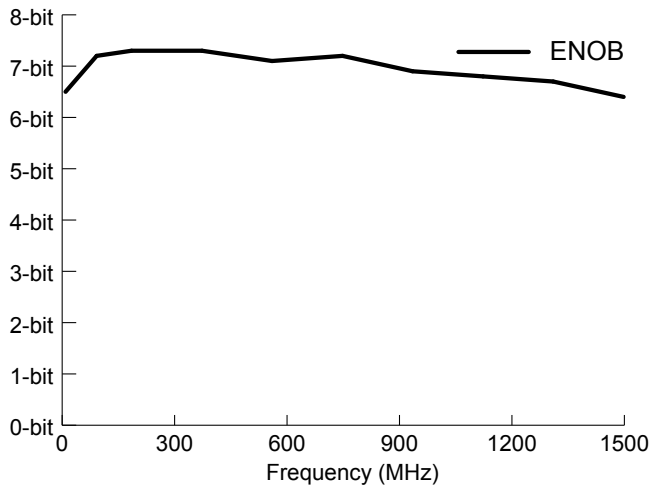
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Figure 1: Typical wide bandwidth response (contact Curtiss-Wright for more information)



### Clocks, Triggers & Multi-board Sync

The AD1500 provides a front-panel MMCX connector for connecting an external sample clock source (required). A front panel mounted trigger input (TI) and a trigger output (TO) signal are connected to the FPGA via LVPECL I/O stages. This allows the FPGA to define the trigger mechanism for the application for maximum flexibility.

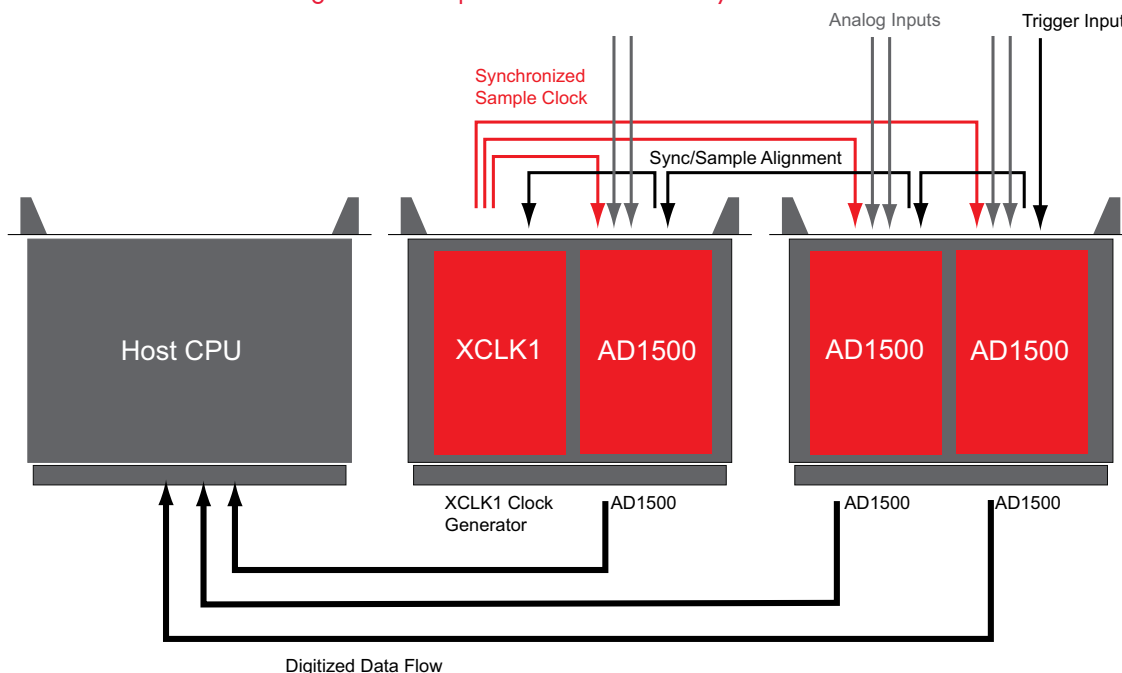
The AD1500 supports multi-board synchronization allowing all ADCs to be synchronized to a common clock source. When synchronized, all data will be aligned and coherent across multiple AD1500 boards. Curtiss-Wright's XCLK1 clock generator is capable of providing this synchronized sample clock output to two or more AD1500 ADCs, providing support for features such as synchronous reset of the sample clock.

### Xilinx Virtex-5 FPGA

The AD1500 is fitted with a Xilinx Virtex-5 SX95T FPGA (contact Curtiss-Wright for availability of other FPGA variants) which is optimized for a high ratio of DSP blocks to standard logic blocks to support high performance signal processing.

The FPGA is configured at power up from FLASH with a default image, a recovery image or an image the customer generates. In addition to FLASH configuration, new images can be downloaded from the host via the PCI or PCIe interface. Software is provided to load new images into either FLASH or SRAM. Bit streams stored in SRAM benefit from faster downloads while bypassing non-volatile storage - useful for secure applications.

Figure 2: Multiple AD1500s can be synchronized





### **Multiple SDRAM & SRAM Banks**

The AD1500 features both external SRAM and SDRAM connected to the FPGA. These can be used for buffering ADC data or for general purpose processing support.

The two 128MB DDR2 SDRAM banks on the AD1500 can be used in parallel to buffer digitized data. Each bank is 16-bits wide.

QDR2 SRAM provides higher bandwidth external memory. Two 2M x 36-bit banks are fitted on the AD1500.

### **PCI/PCI-X, PCIe & Multi-GB/s I/O**

The AD1500 includes a PCI/PCI-X interface, supporting up to 133MHz operation, and a PCIe interface. These interfaces provide multi-channel DMA support.

The PCIe interface uses the Virtex-5 FPGA's RocketIO™ GTP transceivers and an embedded end-point controller. The Virtex-5 FPGA provides sixteen, full duplex high-speed serial communication links through RocketIO GTP transceivers. These links are evenly split between two XMC (VITA 42) connectors. Each link is able to operate at up to 3.2GB/s (using an SX95T FPGA) and can be driven as independent data streams or bonded to create 'fat pipes' for fewer, but higher bandwidth, data streams. A built-in PCIe end-point block allows x4 or x8 lane communications at 2.5GB/s. This is a hard IP block within the Virtex-5 FPGA, which can be bypassed for other protocols such as sFPDP.

### **Rugged Build Options**

A range of environmental requirements are addressed by the AD1500: air-cooled benign, air-cooled extended temperature, air-cooled rugged and conduction-cooled. For conduction-cooled applications, the host board must be able to incorporate front panel I/O connections. Depending on the application, a suitable heatsink may be required for conduction-cooled builds.

### **FusionXF Software/HDL Support**

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities with examples and infrastructure for using the AD1500 or the AD1500 on one of Curtiss-Wright's other Xilinx Virtex-5 and Virtex-4 FPGA-based products. This includes a C-API and sophisticated DMA support.

One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA. FusionXF makes HDL development easier and integration more straightforward.

Example software/HDL illustrates how to interface to on-board devices such as QDR SRAM and DDR SDRAM. Under software running on the host, data can be moved to and from the AD1500's memories using FusionXF's high performance DMA capabilities.

Software utilities are provided for configuring the FPGA. These include FLASH programming and commands to configure the FPGA from a given image in FLASH or SRAM. The FPGA may also be configured via a ChipScope™ Pro/JTAG interface. Host operating systems supported by the FusionXF suite includes Windows, VxWorks and Linux.

Although the AD1500 is aimed at applications requiring both high-speed digitization and user programmable FPGA processing, an acquisition-only example image is provided. This allows the AD1500 to be used 'out-of-the-box' without having to develop FPGA code. This image can be loaded from the FLASH file system and supports full bandwidth data acquisition, external trigger modes and high-speed DMA driven PCI-X/PCIe channels to the host processor. This example can be modified to include a user application, making the AD1500 quick and easy to use.

Please contact your Curtiss-Wright representative for an AD1500 characterization report.



Figure 3: AD1500 Block Diagram

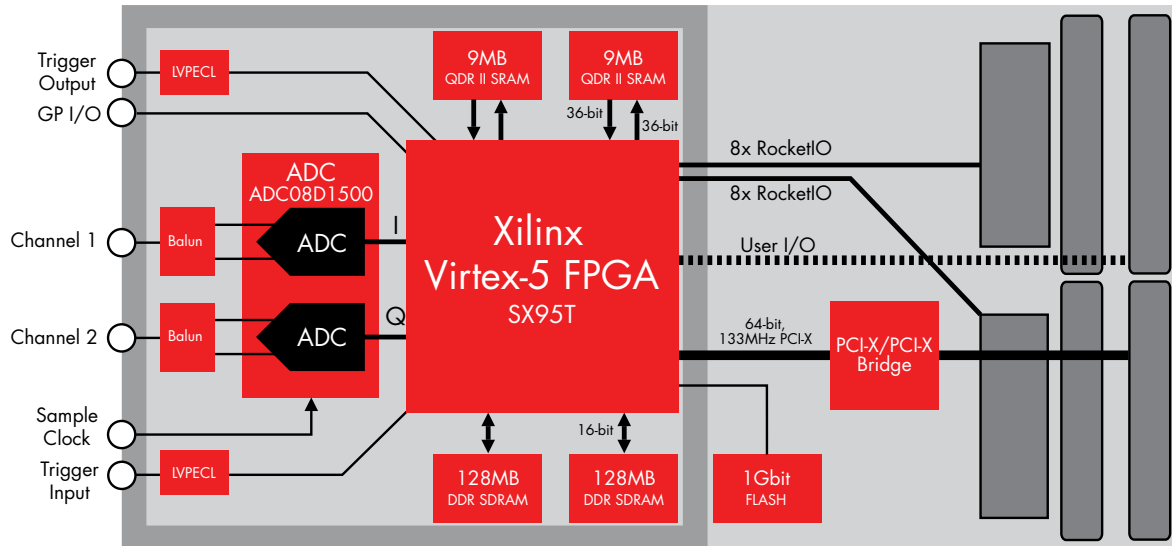


Table 1: Specifications

FPGA	
Device	Xilinx Virtex-5 SX95T (speed grade 2)
DDR2 SDRAM	2 banks of 64M x 16-bit (2 banks of 128MB)
QDR2 SRAM	2 banks of 2M x 36-bit (2 banks of 9MB)
FLASH	1 Gbit (FPGA boot/configuration including rescue image)
Analog Input	
Number of Channels	2, single-ended
Sampling Frequency	Up to 1.5GSPS
Full Scale Input Voltage	600-800 mV (programmable)
Device	ADC08D1500
Full Power Bandwidth (3dB)	1.5GHz
Input Impedance	50 Ohm, AC coupled
SNR (device)	46 dB <sup>1</sup>
SFDR (device)	57 dBc <sup>1</sup>
ENOB (device)	7.3 bits <sup>1</sup>
Clock & Trigger Inputs	
External	Front panel MMCX
Input Level	600-1800mV (sine or square wave)
Sample Frequency Range	200MSPS to 1500GSPS
Input Impedance	50 Ohm, AC coupled
Trigger Input/Output	Single-ended, 50 Ohm, LVPECL, DC coupled

PCI	
PCI Compliance	32/64-bit PCI 33MHz, PCI-X 66/100/133MHz, Master/slave/DMA, Interrupt support
XMC (3.3V only)	
XMC P15	8x RocketIO @ 3.125GB/s or 8x PCIe
XMC P16	8x RocketIO @ 3.125GB/s
Software/HDL Code	
Host Drivers	Windows, VxWorks 6.x, Linux
Utilities	FLASH programming, diagnostics
Software/HDL Code	Analog input, memory interfaces, PCI-X, PCIe
Miscellaneous	
Weight	TBD

Notes

1. Representative figures, not guaranteed at 373MHz



**Table 2:**  
**Environmental Specifications**

		Commercial	Rugged	
			Air-cooled	Conduction-cooled
			Level 100 <sup>1</sup>	Level 100 <sup>1</sup>
Temperature	Operational (at sea level)	0°C to +55°C (15 CFM air flow) <sup>2</sup>	-40°C to +70°C (20 CFM air flow) <sup>2</sup>	-40°C to +70°C (Card Edge Temp) <sup>3</sup>
	Non-Operational	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C
Vibration	Operational (Random)	-	0.04g <sup>2</sup> /Hz	0.1g <sup>2</sup> /Hz
Shock	Operational	-	30g peak, 11ms half sine	40g peak, 11ms half sine
Humidity	Operational	5-95% non-condensing	Up to 95%	Up to 95%
Altitude <sup>4</sup>	Operational	-	-1,500 to 60,000ft	-1,500 to 60,000ft
Conformal Coating <sup>5</sup>		No	Yes	Yes

**Notes**

1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate should be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA. (ref. <http://humiseal.com> for details)

\*While the AD1500 is designed to meet these environmental requirements, formal qualification testing has not been performed to these levels. Please contact your local sales representative to discuss your program specific requirements.

**Warranty**

This product has a one year warranty.

**Contact Information**

To find your appropriate sales representative, please visit:

Website: [www.cwembedded.com/sales](http://www.cwembedded.com/sales)

Email: [sales@cwembedded.com](mailto:sales@cwembedded.com)

For technical support, please visit:

Website: [www.cwembedded.com/support1](http://www.cwembedded.com/support1)

Email: [support1@cwembedded.com](mailto:support1@cwembedded.com)

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