# TN-20: DTA-3290 – A Complete Software Defined Radio with Tunable RF Transceive Front End Up To 6GHz

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## Introduction

A complete Software Defined Radio (SDR) requires requires a very flexible RF front end to handle the tunability and frequency agility demanded by SDRs. The DTA-3290 is a versatile single channel complete SDR solution with an extremely flexible RF front end coupled with a 16-bit ADC and DAC channel. Like all D-TA products, the DTA-3290 comes with a 10GbE network for easy connectivity to a server for real time software processing. The 10GbE interface allows processing of the full 40 MHz instantaneous bandwidth with the aid of high performance SDK available from D-TA.

The DTA-3290 is ideally suited for a variety of single channel applications like SIGINT, COMINT, communications, arbitrary waveform generator, distributed TDOA, Radar, Sonobuoy, HF/VHF/UHF Modem, RF Test and measurement etc. The DTA-3290 can seamlessly operate with our record/playback systems providing a very versatile solution.

## System Architecture

The simplified block diagram of the DTA-3290 is shown in Figure 1. The DTA-3290 comprises of two major building blocks: <i> RF Section with a single channel Up Converter (UCON) and Down Converter (DCON) <ii> Digital IF section with a 16-bit ADC and DAC with a large Virtex 5 FPGA and 10GbE link for high speed data transfer and 1GbE link for control. The DTA-3290 is a 19” rackmountable unit, 1U high and 20” deep. Other customized packaging options are also available.

***Major Features:***

- Separate UCON & DCON synthesizers for independent receive and transmit
- 16-bit ADC and 16-bit DAC optimized for operation with the RF front end
- Large Virtex 5 (SX95T) FPGA
- Programmable DDC (decimation: 2, 4, 8, 26, 32) for optimal bandwidth selection
- 10GbE Network for full transceive operation with 40 MHz instantaneous BW
- 1GbE link for command and control

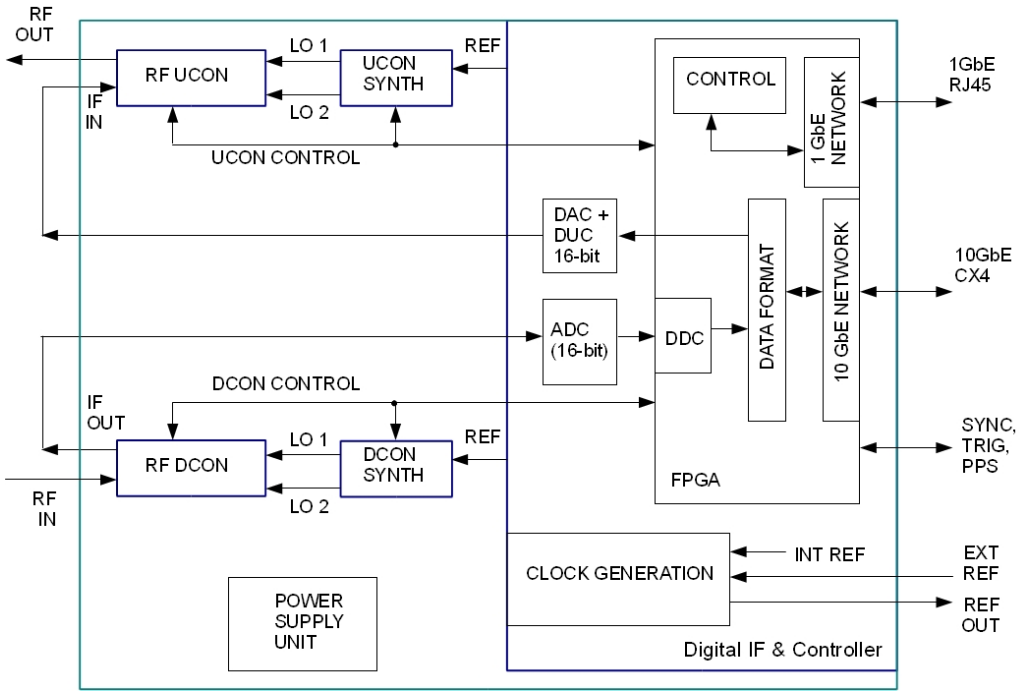


*Figure 1: System Block Diagram of the DTA-3290*

## *Added Features that makes DTA-3290 ideal for a variety of applications*

***RF Input / Output Switch Matrix*:** This enables a seamless scanning operation by enabling users to connect to multiple antenna (or power amplifiers) to enable frequency coverage up to 6 GHz.

***Front-End LNA or Attenuator*:** The receiver input path architecture allows users to switch in either an LNA (for low signals) or a programmable attenuator (for large signal scenario). This allows users to make a Noise Figure vs. IP3 tradeoff and prevent saturation of amplifiers and mixers in the presence of large signals.

***LNA Out & Pre-Amp In Ports:*** The front end LNA output and the Pre-amp inputs are externally accessible for handling variety of inputs and adding customized filtering.

***Digital Programmable Attenuators*:** Up to three (3) programmable attenuators (1 dB steps) are available for users to calibrate gain over the 6GHz frequency range of operation. These attenuators are also used for programmable gain control.

***Integrated ADC & DAC***: By integrating the ADC and the DAC in the unit, the users are spared the system integration issues. The RF UCON and DCON are designed to operate with the high performance ADC and DAC and all requisite gain and filtering is integrated. All ADC and DAC clocks required to undersample the IF signal are provided and are optimized for sampling the IF from the RF UCON and DCON modules.

***10GbE Network for fastest data transfer*:** Like all D-TA products, the DTA-3290 implements a 10 GbE nework for high speed data transfer to a DTA-1000 server for real time recording and processing.

## *RF Down Converter (DCON)*

The simplified block diagram of the RF down converter is shown in Figure 2. The RF front end has an antenna switch built in that allows the user to connect two band specific antenna covering the entire frequency range (20 to 6000 MHz) and scan the entire band without switching antenna. Alternately, the second input port can be used as a test port for in-line calibration. The front also features a design that allows the user to choose between a high gain, low noise figure (high sensitivity) mode or a low gain, high IP3 (LNA bypassed) mode. This selection is software selectable. An external loopback of the LNA and pre-amp stage allows users to add additional pre-selector filters. D-TA Systems can also supply any customized pre-selection filters. Please contact factory for more details. The DCON features four preselector filters that provide the required image rejection and three programmable attenuators that allow the user to control the gain. In the high sensitivity mode only two programmable attenuators are available. A two stage conversion process is utilized with a final IF frequency of 75 MHz. This allows the best possible sampling option with the ADC running at 100 MHz sampling rate. The DTA-3290 API (full source code available) allow ease of control and selection of proper RF path.

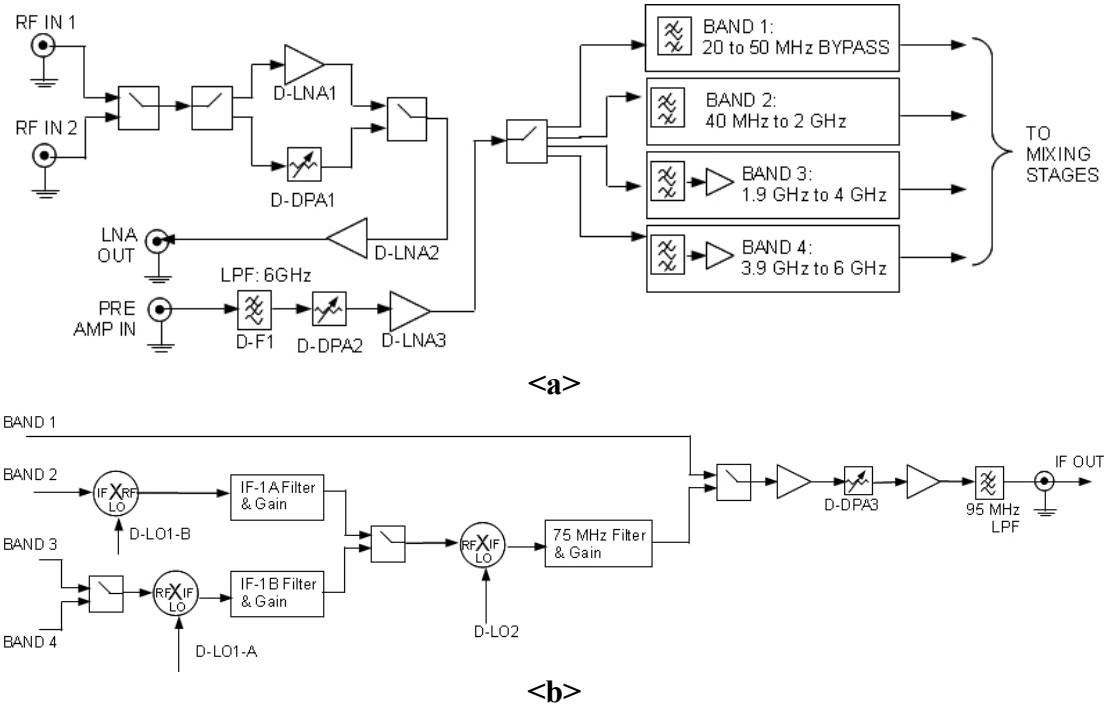


*Figure 2: DTA-3290 RF Down Converter (DCON) simplified block diagram. <a> shows the front end of the DCON and <b> shows the back end*

The DCON RF bands are shown in Table 1.

*Table 1: DCON RF Bands*

| BAND NUMBER | DCON FREQUENCY COVERAGE |
|---|---|
| 1 | 20 to 55 MHz (Direct path, no conversion) |
| 2 | 40 to 2000 MHz |
| 3 | 1960 to 4000 MHz |
| 4 | 3960 to 6000 MHz |

There is 40 MHz overlap between the bands (other than Band 1 and Band 2). A two stage down conversion is employed for providing the optimal performance. The last mixing stage (D-LO2) provides an option to flip the spectrum.

## *RF Up Converter (UCON)*

The simplified block diagram of the RF down converter is shown in Figure 3. The up conversion is accomplished via a two stage conversion process. The first mixing stage converts the signal to a fixed internal IF. This stage offers the option of spectrum flip. The second mixing stage converts the signal to the desired RF band and the RF band select filters filter the other mixing products.

There are eight (8) RF paths including one bypass path (without any conversion). The RF bands for the UCON is shown in Table 2.

*Table 2: UCON RF Bands*

| BAND NUMBER | FREQUENCY COVERAGE |
|---|---|
| 0 | 55 to 95 MHz (Direct path, no conversion) |
| 1 | 20 to 1320 MHz |
| 2–1 | 1280 to 2000 MHz |
| 2–2 | 1960 to 2470 MHz |
| 2–3 | 2430 to 2920 MHz |
| 3 | 2880 to 3670 MHz |
| 4–1 | 3630 to 5000 MHz |
| 4–2 | 4960 to 6000 MHz |

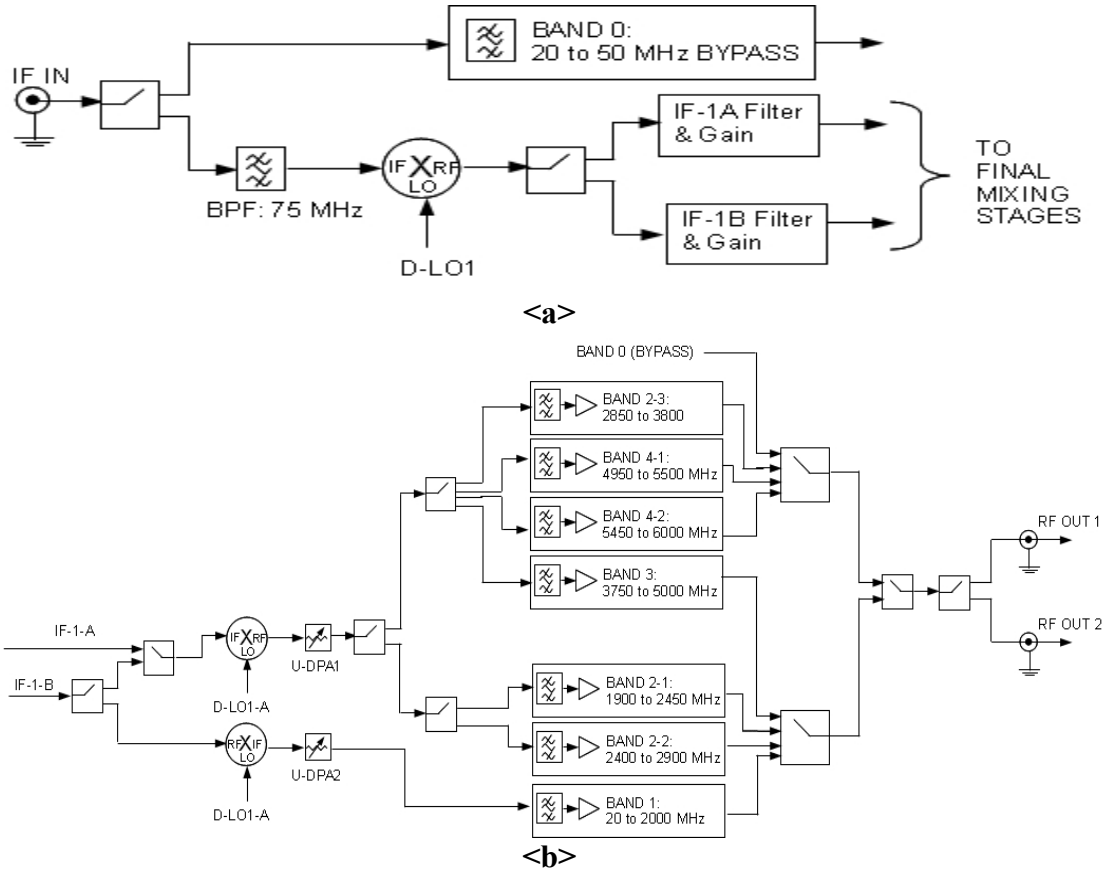


*Figure 3: DTA-3290 RF Up Converter (UCON) simplified block diagram. <a> shows the path till the first mixing stage and <b> shows the second mixing stage followed by the band select filters*

## *Digital IF*

The Digital IF section includes 16-bit ADC and DAC directly connected to a large Virtex 5 SX95T FPGA. The FPGA implements a programmable DDC and all 10GbE and 1GbE network logic. The 10GbE link is implemented as a CX4 copper link for full bandwidth data transfer to a multi-core server for real time processing. D-TA supplies a multi-threaded Software Development Kit (SDK) for real time application development. Please refer to TN-14 for more information.

The simplified block diagram for the digital IF section is shown in Figure 4. the Digital IF section reuses our DTA-2210 product. More more information please refer to TN-04 (“Getting to Know the DTA-2210).

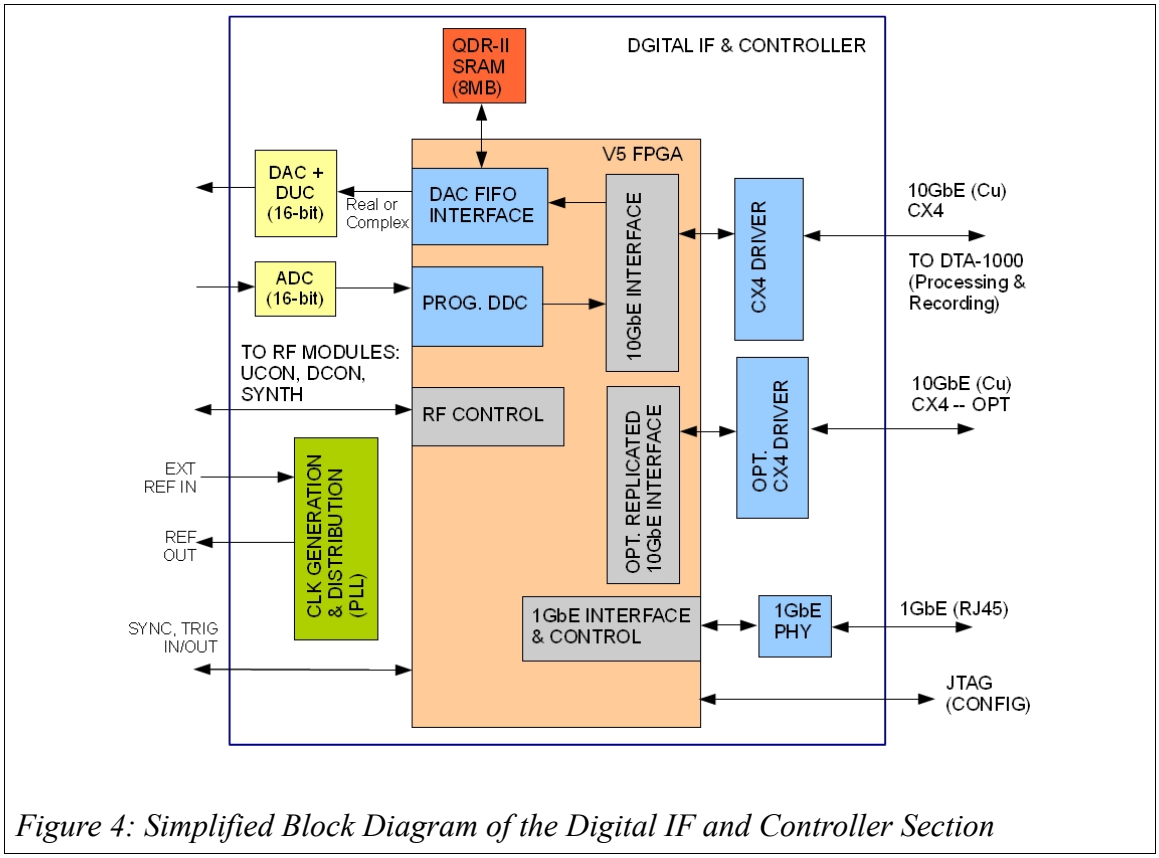


*Figure 4: Simplified Block Diagram of the Digital IF and Controller Section*

The programmable DDC implemented in the FPGA allows decimation factors of 2, 4, 8, 16 and 32. The filter taps are also programmable by the user. The DDCs baseband the digitized IF signal and produces a complex (I & Q) output as shown in the spectral sketch in Figure 5. The baseband complex signals are sent via the 10 Gigabit network for further processing by the server. The DDC allows the user to reduce the processing bandwidth and thereby reduce the data rate. The ADC is programmed to operate at 100 MSPS and can very easily undersample the 75 MHz IF coming out of the RF DCON section. The SAW filters in the RF section serves as anti-alias filters and further filter is not required.

The DAC includes programmable interpolation and upconversion feature and thus allows the user to provide complex baseband data. The compelx baseband data can be upconverterd to a 75 MHz IF and fed to the RF UCON section. The RF UCON input section provides the reconstruction filters and attenuates the images created in the DAC. The DAC may also be operated in the real mode.

The ADC and the DAC sections are very similar to the DTA-2300, the multi-channel IF transceiver. Please refer to TN-04 and TN-05 for more information.

The FPGA also acts as the controller for the UCON, DCON and the SYNTH modules of the RF section. The host computer connects to the DTA-3290 via the 1GbE link and the API simplifies system integration.

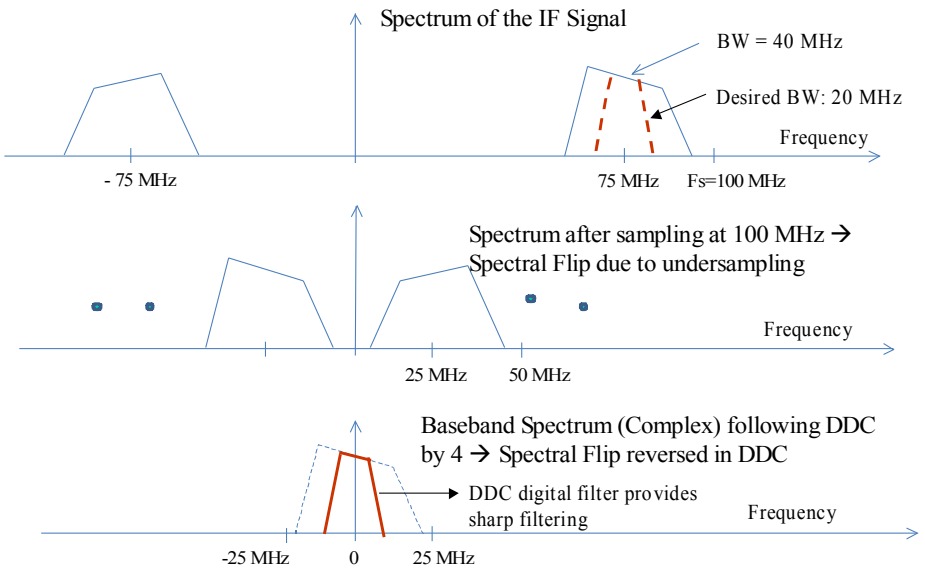


*Figure 5: Illustration of receive signal processing for 20 MHz BW. For receive processing the undersampled signal is converted to complex baseband signal by the DDC. The programmable decimation of the DDC selects the desired bandwidth.*

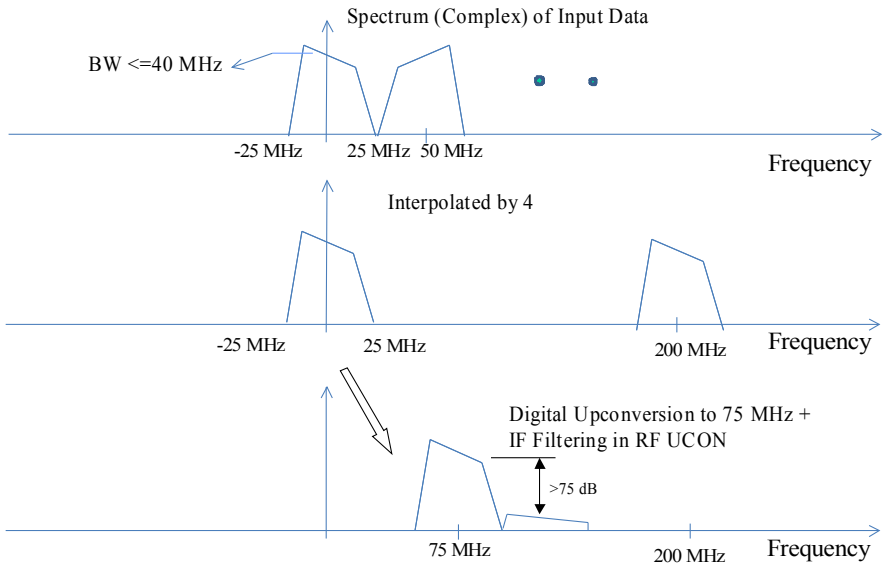


*Figure 6: Illustration of transmit signal processing for 40 MHz BW. For transmit processing the complex baseband data is first up converted to 75 MHz IF for RF conversion using only the real part at the DAC output.*

### *Clock & Reference*

The DTA-3290 implements a very flexible clock generation architecture. For a stand-alone operation the internal TCXO (100 MHz) produces the reference signal that is used to generate all the LOs required for the conversion stages. The TCXO also produces the ADC and DAC clocks. The IF frequency of the RF UCON & DCON are at 75 MHz and are optimized for the 100 MHz sampling clock. The IF section has a programmable clock generation section that allows the user to create other sampling clocks for customized operation.

## Programming Interface and API support

The DTA-3290 can be programmed over a 1GbE interface (copper). The software development kit contains extensive API functions that allow the user to control the RF unit. The SDK also allows the user to very easily integrate the control functionality of the DTA-3290 into user applications.

## Major Specification

| FEATURES | VALUE | COMMENTS |
|---|---|---|
| ***RF*** | | |
| Number of Transceiver Channels | 1 | Transmit and Receive channels can be tuned to different channels. Simultaneous Transmit and Receive operation. |
| RF Input Switch Matrix | 2:1 | Two RF antenna input ports provided. Can be used for automatic antenna switching or on-line calibration |
| RF Output Switch Matrix | 1:2 | Two RF antenna output ports provided. Can be used for automatic antenna switching or on-line calibration |
| Frequency Coverage | 20 MHz to 6 GHz | Up and Down Conversion . Synchronized (i.e. all channels tuned to the same frequency). Transmit and Receive tuning frequencies can be different. Contact factory if independent tuning required on all channels. |
| Instantaneous BW | 40 MHz | Transmit and Receive. Smaller bandwidth possible with built in DDC |
| IF Output (DCON) | 75 MHz | Centre Frequency. Sampled with the ADC at 100 MSPS |
| IF Input (UCON) | 75 MHz | Centre Frequency. Created with the DAC/DUC |
| Number of Receive Sub-bands | 4 | 20 to 50 MHz (Bypass, no conversion)<br>40 to 2000 MHz<br>1960 to 4000 MHz<br>3960 to 6000 MHz |

| FEATURES | VALUE | COMMENTS |
|---|---|---|
| Number of Transmit Sub-bands | 8 | 55 to 95 MHz (Direct path, no conversion)<br>20 to 1320 MHz<br>1280 to 2000 MHz<br>1960 to 2470 MHz<br>2430 to 2920 MHz<br>2880 to 3670 MHz<br>3630 to 5000 MHz<br>4960 to 6000 MHz |
| Receive Gain | 50 dB | Attenuators can be used by the user to compensate for gain variation with frequency |
| Receive Gain Control | 62 | Two 31-dB attenuator for High Sensitivity case. Large signal mode has an extra 31-dB attenuator. All attenuators controllable in 1-dB steps. |
| Receive Noise Figure | < 8 dB | At Maximum Gain in High Sensitivity Mode |
| Receive OIP3 | > +30 dBm | Typical |
| Receive Image Reject | 80 dB | Typical |
| IF Output Power (DCON) | 0 dBm | Typical. At maximum Gain |
| RF Output Power (UCON) | 0 dBm | With 0 dBm IF signal created in baseband |
| Transmit Image Reject | 60 dB | |
| Up converter spurious | -60 dBc | With 0 dBm RF output |
| VSWR | 2:1 | RF In and RF Out ports. This represents 9.5 dB RL |
| Synthesizer Phase Noise | -74dBc/Hz @ 1kHz offset<br>-80 dBc/Hz @ 10kHz offset<br>-94 dBc/Hz @ 100 kHz offset | |
| Tuning Speed | 1 ms | Faster options available. Contact factory for details |
| Tuning Resolution | 200 kHz | Finer tuning performed by DTA-2300 (Digital IF Platform) |
| ***DIGITAL IF*** | | |
| Number of ADC | 1 | |
| Number of DAC | 1 | Real or Complex mode possible. If complex mode used, then the real portion is provided to the RF UCON section |
| Precision | 16-bits | ADC & DAC |
| DDC Decimation | 2, 4, 8, 16, 32 | Programmable. Implemented in the FPGA. |
| DUC interpolation | 2, 4, 8 | Programmable. Bypass possible. Integrated with the DAC |

| FEATURES | VALUE | COMMENTS |
|---|---|---|
| ADC Sampling Rate | 100 MSPS | Ideal for sampling 75 MHz IF from RF DCON |
| DAC Data Rate | 100 MSPS real or 50 MSPS complex | Captured ADC or DDC data can be directly played back. Built in interpolation and up conversion allows creation of 75 MHz IF |
| ADC SFDR | <-85 dBFS | |
| DAC SFDR | <-70 dBFS | |
| Data Transfer to Host | 10 GbE (Copper over CX4) | One 10GbE port available in standard configuration. A replicated port is available as an option. |
| ***ENVIRONMENTAL*** | | |
| Operating temperature | 0 to +50C | Ambient |
| Area of Use | Indoor | |
| Air Flow | Provided by internal fans | User must provide adequate air flow over the chassis. The chassis serves as heatsink |
| ***MISCELLANEOUS*** | | |
| Control | 1 GbE | Copper RJ-45 connector |
| SDK | Available | Contains API. Full source code for integrating into user's application |
| Reference | Internal or External | Internal Frequency is available to the user |
| Internal Reference Frequency | 100 MHz | Will work with a 10 MHz external reference. |
| Dimension | 17.2” (W) x 20” (D) x 1.75” (H) | 1U high, 19” rackmountable, 20” deep |

## Performance

Extensive performance characterization plots are provided in the Appendix. Of particular interest are Figure 10, Figure 11, Figure 16 and Figure 17 which show the sensitivity of the DTA-3290 receiver. Transmitter performance is shown in Figure 18 To Figure 22.

## Ease of Application Development

The 10GbE network allow the DTA-3290 to easily transfer full bandwidth data to a server (DTA-1000) for intelligent recording and real-time processing. The DTA-1000 is a multi-core server with two quad core processors and integrated with the 10GbE NIC and installed with all system software and SDK required implementing real time applications. This allows another level of system integration that allows rapid prototyping and deployment. The appropriate SDK is pre-installed and all example codes are ready to run. The DTA-1000 is an extremely cost effective way for rapid prototyping and quick deployment. The DTA-1000 is optionally available with up to 8 TB of storage for

recording a 40 MHz bandwidth signal to disk. The recorded signal can be played back with the DTA-3290 transmitter. Alternately, user created files can be played back for an extremely flexible arbitrary waveform generator.

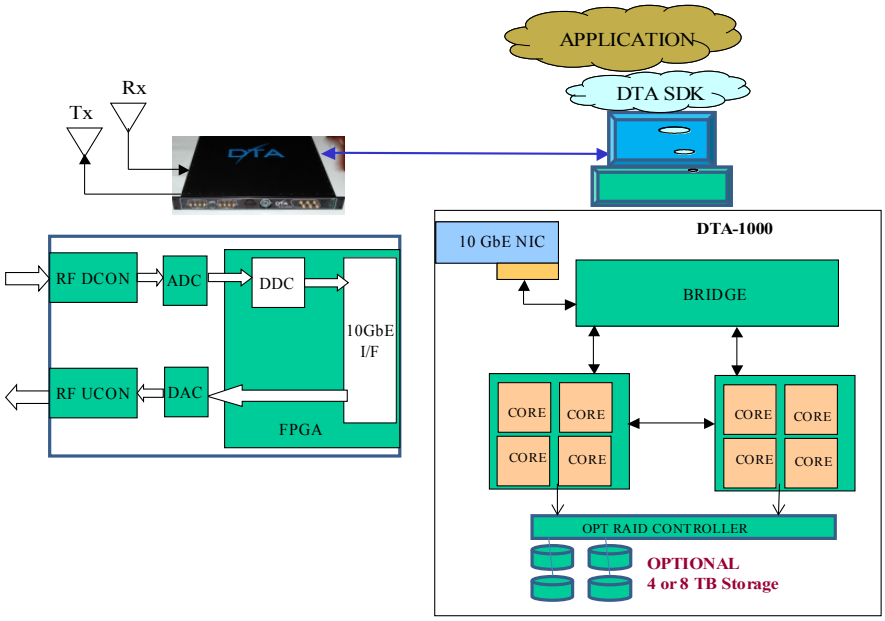


*Figure 7: The SDK allows the user to concentrate on specific application code without worrying about system integration issues. The DTA-1000 is an integrated server with 10GbE NIC and optional storage for sustained recording of 40 MHz bandwidth RF signal. The DTA-1000 will also support intelligent recording.*

D-TA Systems also offers application development support for quick deployment utilizing our expertise in multi-threaded, multi-core software development expertise. Our expertise and the Software Development Kit (SDK) simplifies easy development of real time processing modules for today's high performance multi-core servers. The SDK allows users to harness the immense and ever-increasing processing power of servers, and enables users to develop applications that are scalable with server performance, thereby keeping ahead of the obsolescence curve. For more information on real time processing of 10GbE data please refer to TN-14 for more information.

## Distributed Processing: TDOA

The DTA-3290 is ideally suited for distributed Time Difference of Arrival (TDOA) processing (see Figure 8). The DTA-3290 is equipped with a programmable VCO that can be synchronized to an external reference. This external reference can in turn be synchronized to a common time base such as GPS. The GPS synchronized reference can also be used to lock the LOs in the RF path. The DTA-3290 also accepts an external

trigger, which can again be locked to the external reference (e.g. a GPS 1PPS). This technique allows one to set up the synchronized operation of multiple DTA 3290 units spread out over a large distance.

Typical TDOA systems are often limited by their ability to transfer data between the data acquisition front-ends and the geo-location processor. An option, that allows for a reduction in the intra-system communication bandwidth, is to pre-process the data at the front-end. The DTA-3290 offers the TDOA system designer the best of both worlds. The built-in 10 Gigabit Ethernet interface and dual Gigabit Ethernet interfaces offer unsurpassed data communication bandwidth. The onboard Virtex-5 FPGA provides massive compute horsepower. Whether your algorithm relies on high data throughput or large amounts of front-end processing, the DTA-3290 is the answer for you.

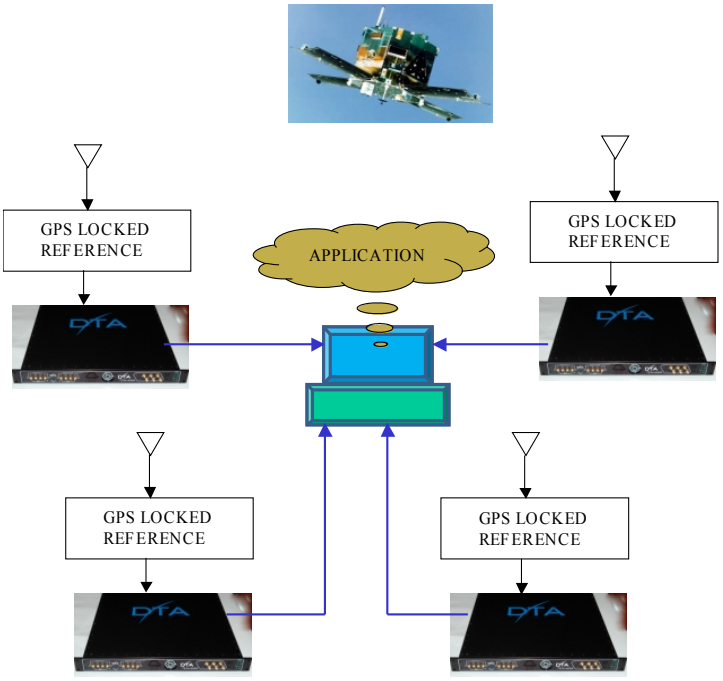


*Figure 8: Distributed processing for Applications like Time Difference Of Arrival (TDOA) processing for direction finding*

## Sample API functions

The API functions available in the DTA-3290 API is provided below as example. We continually add more functions to make the product better.

- void printSystemProperties()
- int regDump()
- int regDump(char *)

- int Init()
- int setSynthPower(RF_CONVERTER_SEL converter, int state)
- int setSynthFreq(RF_CONVERTER_SEL converter, int )
- int setCarrierFreq(RF_CONVERTER_SEL converter, int carrierFreq)
- int setDCONAmplifierPower(int state)
- int setAttenuation(RF_CONVERTER_SEL converter, double attenuation)
- int getUCONState()
- int getDCONState()

## Customization

DTA-3290 can be easily customized to meet specific user requirements. Please contact factory to discuss your specific requirement. More typical customization include:

- Limited band of operation
- Change of IF frequency

D-TA Systems also provides custom RF development capability to meet specific user requirements. They may include low phase noise design, extremely low tuning speed, small form factor design etc.

## Training

We also offer hand-on interactive training either in our fully equipped Training Center or in your facility. The Training Center boasts of a fully equipped conference room and a dedicated Training Laboratory with access to D-TA products as well as test equipment like Oscilloscopes, Spectrum Analyzers, Network Analysers, Signal Generators, etc. The hand-on training cover a full discussion of the SDK structure, detailed product discussions and actual demo application development with actual equipment. The user would be able to create processing applications and determine optimal speed and performance. The specific applications are tailored to meet the user's exact requirement.

We also offer custom application development to meet the users' exact requirement. Please contact us for more information.

## Conclusion

The DTA-3290 is a versatile tunable SDR platform with RF up and down coverter integrated with ADC and DAC. It provides a 40 MHz instantaneous bandwidth with tunability up to 6 GHz. A 10 GbE link allows the digital IF data to be transferred to a server for recording and real-time processing. D-TA provides SDK and application development training to reduce deployment time.

## Appendix A: Performance Plots

The DCON performance plots are shown in Figure 9 through to Figure 17.

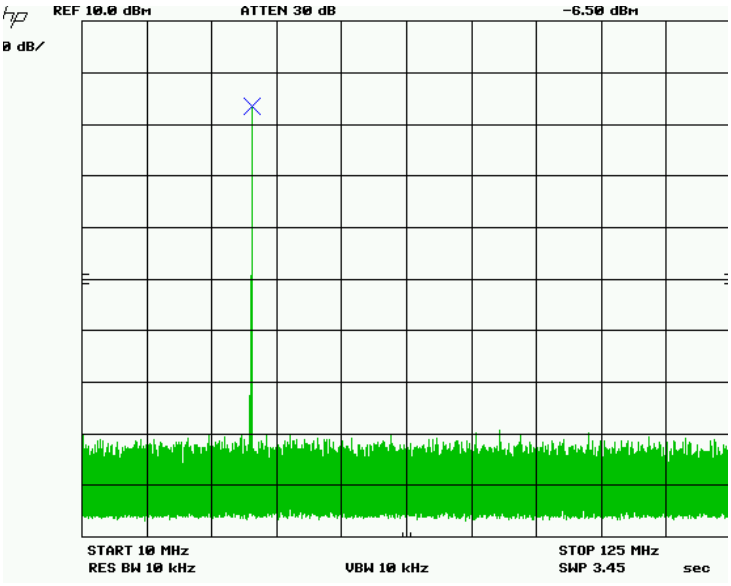


*Figure 9: 40 MHz tone in bypass mode. Input power at -40 dBm, gain of 33.5 dB with front end LNA bypassed*

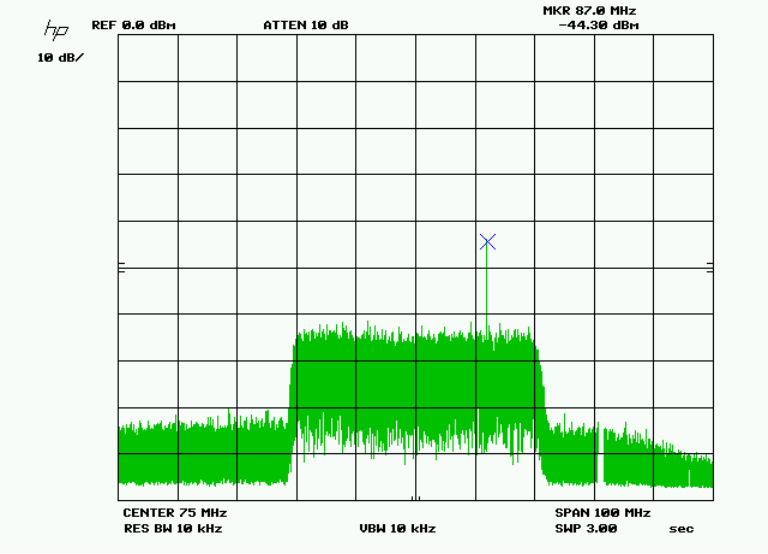


*Figure 10: 3012 MHz tone in at -100 dBm power with DCON tuned to 3 GHz in high sensitivity mode. The output level is -44.3 dBm at 87 MHz for a gain of about 56 dB.*

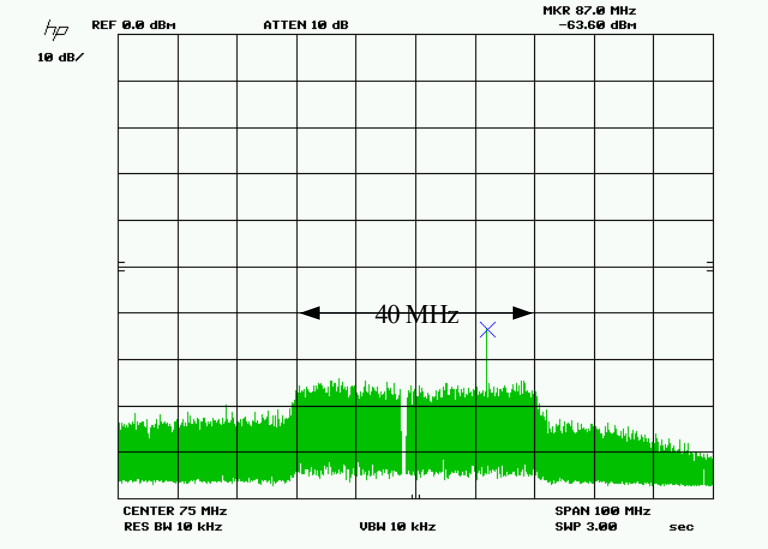


*Figure 11: 3012 MHz tone in at -100 dBm power with DCON tuned to 3GHz in LNA bypassed. The output level is -63.6 dBm at 87 MHz for a gain of 36 dB.*

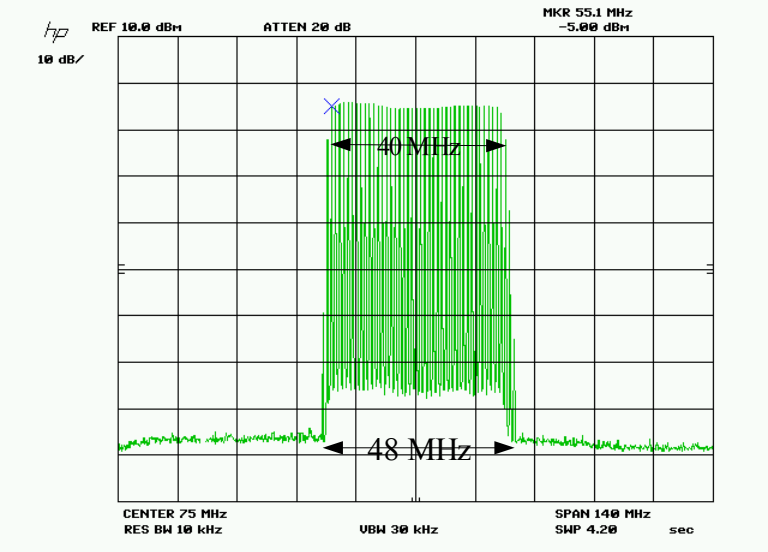


*Figure 12: RF frequency sweep with DCON tuned to 3950 MHz in high sensitivity mode. The RF sweep was from 3880 MHz to 4020 MHz at an input level of -55 dBm. The output level is -5 dBm and flat across the IF output. The gain is about 50 dB.*

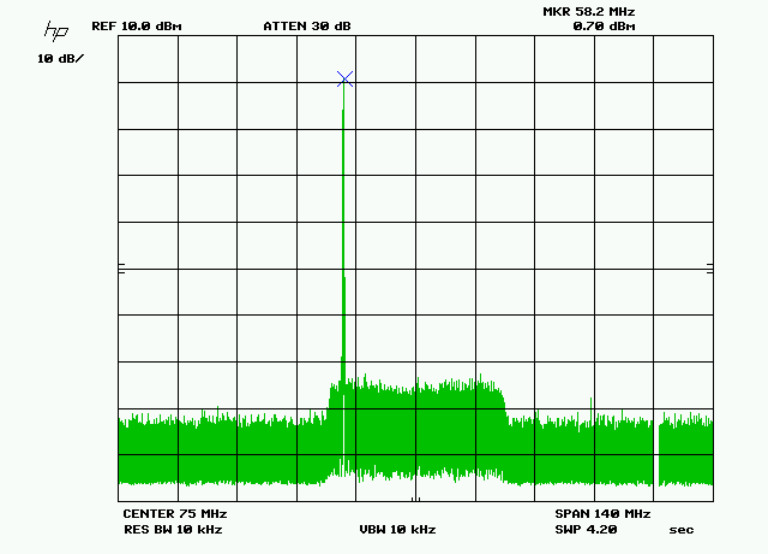


*Figure 13: 1883 MHz tone in at -55 dBm power with DCON tuned to 1900 MHz in high sensitivity mode. The output level is 0.7 dBm at 58 MHz (17 MHz below 75 MHz) for a gain of about 56 dB.*

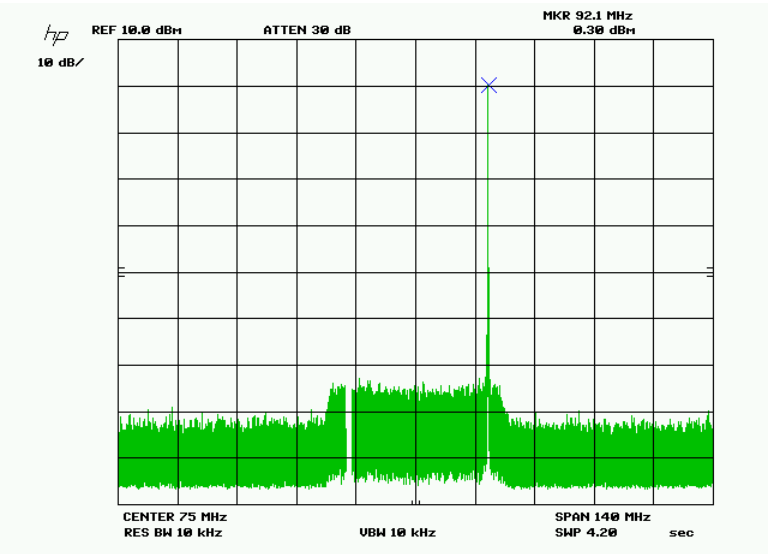


*Figure 14: 1917 MHz tone in at -55 dBm power with DCON tuned to 1900 MHz in high sensitivity mode. The output level is 0.3 dBm at 92 MHz (17 MHz above 75 MHz) for a gain of about 55 dB.*

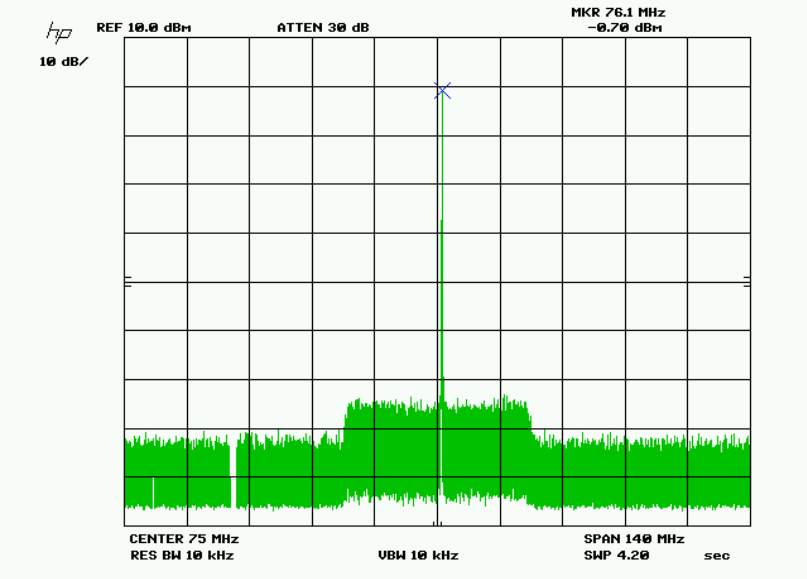


*Figure 15: 1901 MHz tone in at -55 dBm power with DCON tuned to 1900 MHz in high sensitivity mode. The output level is -0.7 dBm at 76 MHz (1 MHz above 75 MHz) for a gain of about 54 dB.*

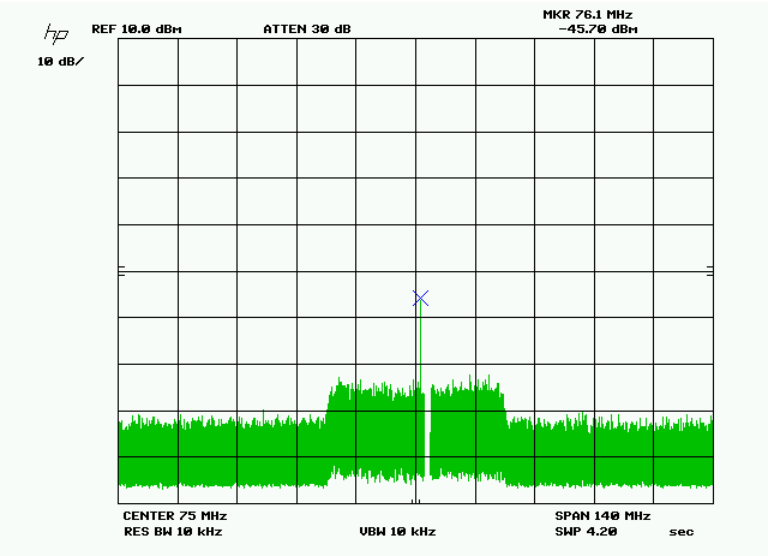


*Figure 16: 1901 MHz tone in at -100 dBm power with DCON tuned to 1900 MHz in high sensitivity mode. The output level is -45.7 dBm at 76 MHz (1 MHz above 75 MHz) for a gain of about 54 dB.*

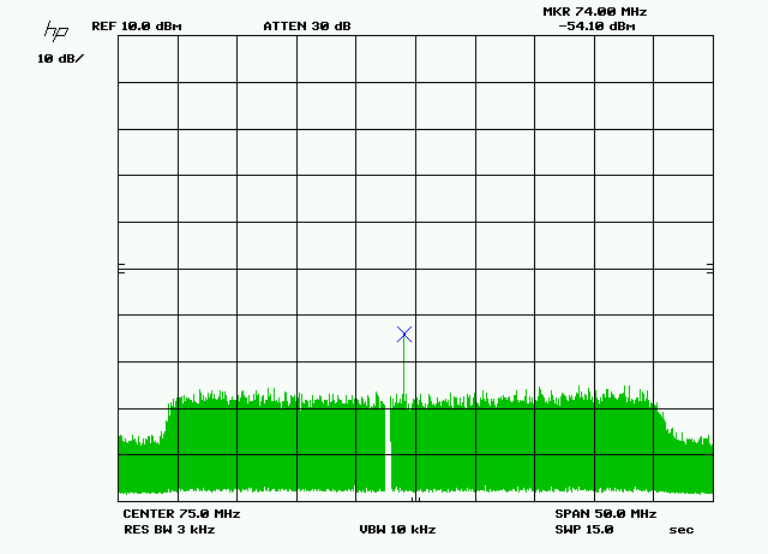


*Figure 17: 1250 MHz tone in at -110 dBm power with DCON tuned to 1251 MHz in high sensitivity mode. The output level is -54.1 dBm at 74 MHz (1 MHz below 75 MHz) for a gain of about 56 dB.*

### *UCON*

The UCON performance plots are shown in Figure 18 through to Figure 22.

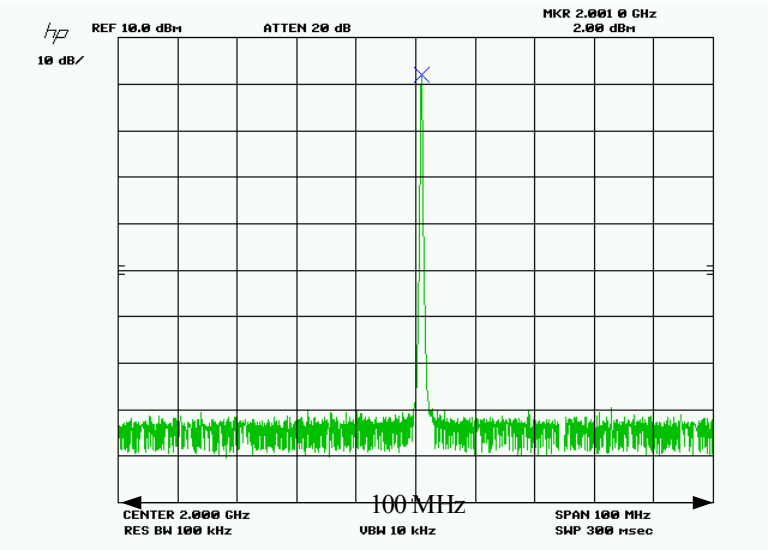


*Figure 18: 76 MHz IF in at -5 dBm power with UCON tuned to 2000 MHz. The output level is 2 dBm at 2001 MHz (1 MHz above the tuning frequency) for a gain of about 7dB.*

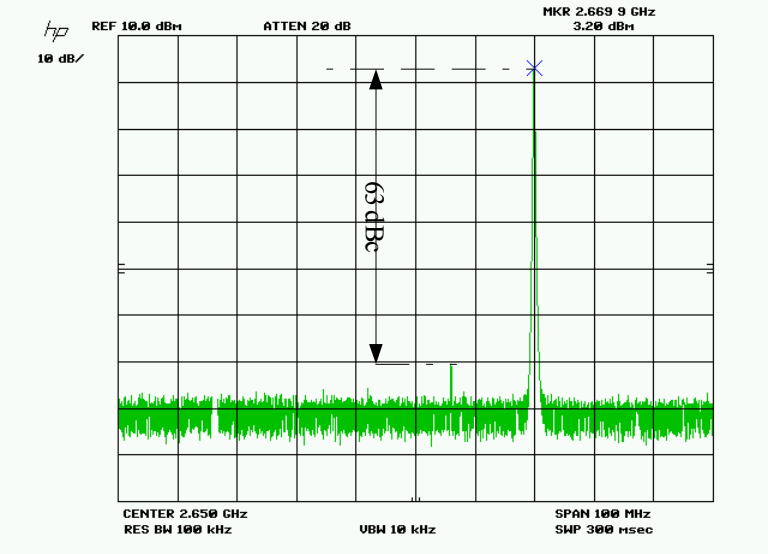


*Figure 19: 55 MHz IF in at 0 dBm power with UCON tuned to 2650 MHz and spectrum flipped. The output level is 3.2 dBm at 2670 MHz (20 MHz above the tuning frequency as the spectrum is flipped) for a gain of about 3 dB.*

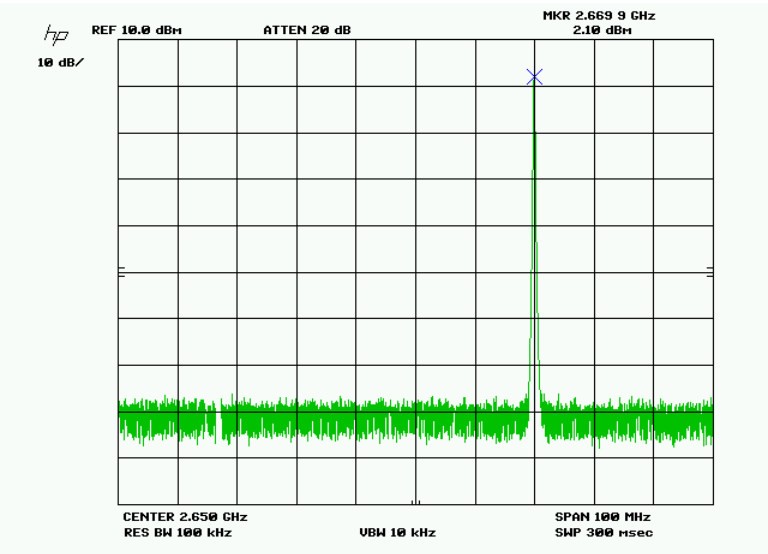


*Figure 20: 95 MHz IF in at 0 dBm power with UCON tuned to 2650 MHz. The output level is 2.1 dBm at 2670 MHz (20 MHz above the tuning frequency) for a gain of about 2 dB.*

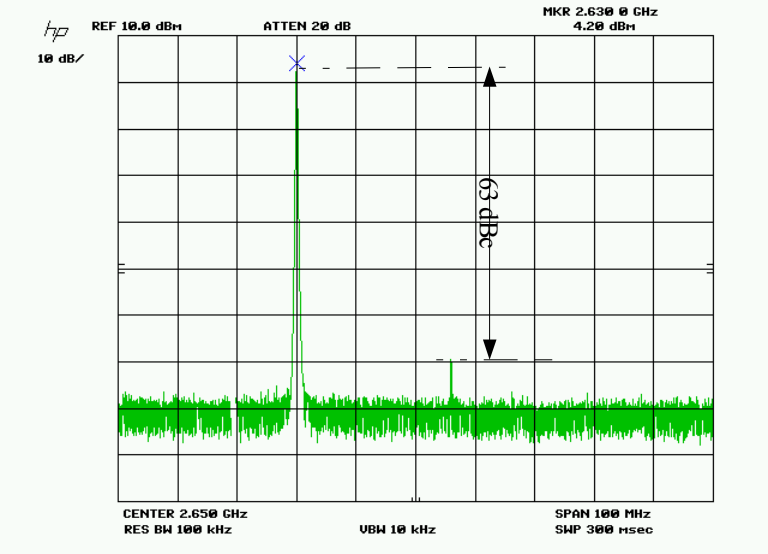


*Figure 21: 95 MHz IF in at 0 dBm power with UCON tuned to 2650 MHz and spectrum flipped. The output level is 4.2 dBm at 2630 MHz (20 MHz below the tuning frequency as the spectrum is flipped) for a gain of about 4 dB.*

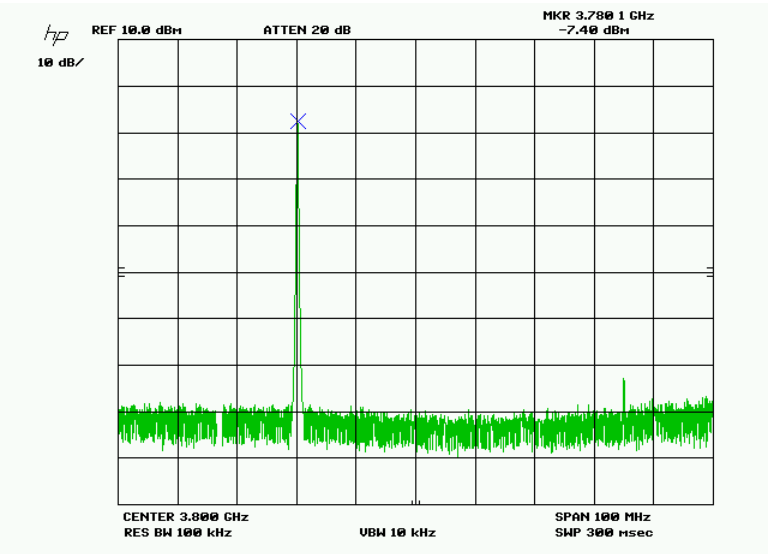


*Figure 22: 55 MHz IF in at 0 dBm power with UCON tuned to 3800 MHz and with 5 dB attenuator. The output level is -7.4 dBm at 3780 MHz (20 MHz below the tuning frequency ) for a total loss of 7.4 dB (including the 5 dB loss in the UCON).*

## Contact Information


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