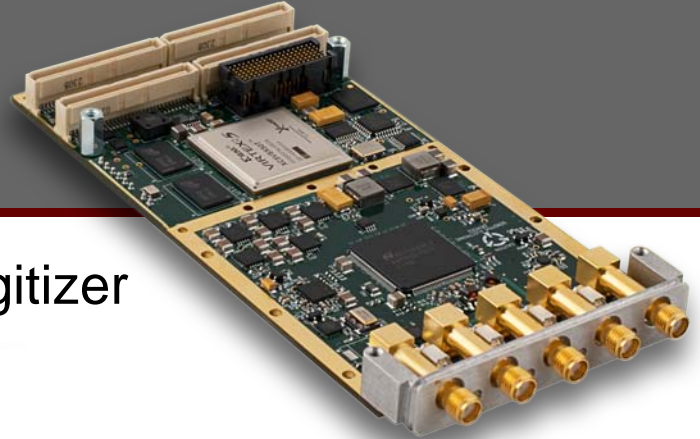




DELPHI

Engineering Group, Inc.

High Performance, Real-Time Acquisition Solutions for the Aerospace, Defense and Communication Industries.



ADX3500 - 3 Gbps XMC/PMC Digitizer

Dual 1.5 Gbps Option / Virtex 5 FPGA

Features

General

- Xilinx Virtex 5 SX50T (FX70T option)
- 8 High-Speed Transceivers @ 3.125 Gbps
- VITA-35 Compliant Pn4 Interface With 32 LVDS Pairs
- 1.7 GHz Full-Power Analog Input Bandwidth
- PCI-X 2.0 Compliant Bus @ 133 MHz
- 64 MB SDRAM Buffer
- VxWorks, Linux, Windows Software Drivers
- PCIe, RapidIO, and Aurora Protocols
- Onboard DMA Engine
- Optional Onboard Clock Via PLL
- VITA 42.3 Compliant
- Conduction/Convection Cooled
- Commercial/Industrial Temperature Ranges
- Compatible With VPX and VXS Host Platforms

Performance

- Analog Input: 100 KHz to 1.7 GHz
- Sampling Rate: 100 Msps up to 3 Gbps
- ENOB = 7.2 Effective Bits, $F_{IN} = 1.5$ GHz
- Low Power Consumption (15 Watts)

Applications

- Radar
- Lidar
- ELINT/SIGINT
- Synthetic Aperture Radar
- Data Analysis Systems
- Preprocessing Systems
- Direct RF Down-Conversion
- High-Speed Test and Instrumentation

Description

Delphi Engineering Group's ADX3500 is an XMC/PMC, analog to digital converter module designed for digitizing wide bandwidth analog signals at 8 bits, at sample rates of up to 1.5 Gbps dual-channel, or 3 Gbps single channel. Samples are transferred via a PCI-X interface or Virtex 5 RocketIO transceivers through an XMC connector. Eight serial transceivers can operate at up to 3.2 Gbps. A PCI Express end-point controller is available within the FPGA supporting x1, x2, x4 or x8 PCI Express operation.

The user-programmable Xilinx Virtex 5 FPGA provides continuous sampling, buffering, and timing. Delphi also offers an FPGA design kit which allows custom development of the onboard FPGA. FPGA design can be customized for specific applications such as digital filtering, data preprocessing and DSP functions such as FFT.

For systems running Microsoft Windows, Delphi offers ADCView, a signal visualization application which displays sampled data graphically. Through ADCView's graphical user interface, users can configure sampling parameters such as: start/stop vectors, IRQ operation, and triggering options. Sample data exportable to analysis applications such as Matlab.

The ADX3500 is has been rigorously tested to operate on leading PowerPC, PC, and DSP host processor systems. Delphi has a proven track-record of delivering high-performance data acquisition modules for mission-critical applications.

Interfaces

Analog Input

Two analog single-ended signals are accepted through SMA female type connectors on the front edge of the module.

Clock Input

An analog single-ended clock input of -10 dBm to +10 dBm is accepted through an SMA female type connector on the front edge of the module. Optional onboard clock provided via PLL.

Trigger Input

Trigger input is provided through an SMA female type connector on the front of the module.

All SMA inputs are 50 ohm terminated.

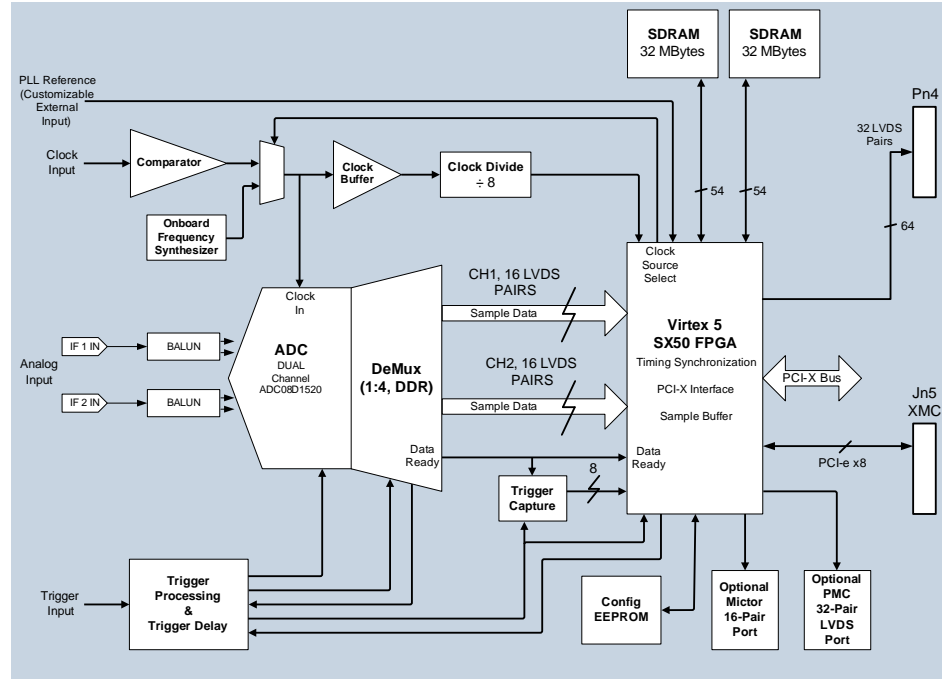
XMC/PCI Interface

Processed sample data is transferred to the host system through the XMC or PCI bus. Data collection timing and duration are fully programmable through the XMC/PCI bus. Both interfaces are implemented in the onboard FPGA.

Onboard FPGA

The board's Xilinx Virtex 5 FPGA implements processing, buffering, timing, DRAM control, and the PCI interface.

Contact factory for custom FPGA design.



Top Level Block Diagram

Analog ADC Performance

- Full Power Analog Input Bandwidth: 1.7 GHz (-3 dBm)
- ENOB = 7.2 Effective Bits, $F_{IN} = 748$ MHz
- SNR = 46.3 dB, SFDR = 53 dB, $F_{IN} = 748$ MHz
- Sampling Rate: 100 Msps to 3 Gps

Environmental Requirements

- Convection Cooled
 - Minimum Airflow: 400 LFM
 - Ambient Air Temp (Commercial): 0°C to +50°C
 - Ambient Air Temp (Industrial): -40°C to +70°C
- Conduction Cooled
 - Cold Wall Temp (Commercial): 0°C to +65°C
 - Cold Wall Temp (Industrial): -40°C to +70°C
- Storage Temperature
 - 55°C to +85°C

Physical Characteristics

- Dimensions: 2.91" x 5.66"
- Weight: 4.6 oz

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