

General Standards Corporation

High Performance Bus Interface Solutions

66-18A08

18-Bit Eight-Output 500KSPS Precision Wideband

PMC Analog Output Board

Available in PMC, PCI, cPCI and PC104-Plus and PCI Express form factors as:

PMC66-18A08:	PMC , Single-width
PCI66-18A08:	PCI , short length
Cpci66-18A08:	cPCI , 3U
PC104P66-18A08:	PC104-Plus
PCle66-18A08:	PCI Express
PCle10466-18A08:	PCle , one-lane on PC/104 form factor

See Ordering Information for details.

Call for availability of other form factors, such as XMC, CCPMC, etc.

FEATURES:

8 Single-ended or 3-Wire Differential 18-Bit Analog Output Channels

Simultaneous Clocking; Individual R-2R 18-Bit DAC per output channel

DC to 500KSPS Sample Rate per Channel; 0-4 MSPS aggregate rate

Output ranges: $\pm 10V$, $\pm 5V$, $\pm 2.5V$, software-selectable

Independent 256K-sample output FIFO Buffer

8 Bidirectional Digital I/O lines; Software-selectable TTL or LVDS compatibility

Internal Sample Rate Generator with 24-Bit rate divider

Hardware Sync and Clock I/O for Multiboard Synchronization; Front-panel and Internal access

Conforms to PCI Bus Specification, Revision 2.3, 66/33 MHz with Universal Signaling

Standard Single-width PMC Form factor

DMA Engine Supports Block-Mode Transfers in Two Channels

On-demand Autocalibration

Integrated DC/DC Conversion and Dual Regulation for Internal Supply Voltages

TYPICAL APPLICATIONS:

- | | | |
|---------------------------|-------------------|-----------------------|
| ✓ Multiple Voltage Source | ✓ Servo Systems | ✓ Waveform Generation |
| ✓ Positioning Systems | ✓ Process Control | |

PRELIMINARY INFORMATION

REV: 081510

FUNCTIONAL DESCRIPTION

The PMC66-18AO8 is a precision 18-Bit analog output product that provides eight simultaneously clocked output channels. Outputs can be clocked at rates up to 500 KSPS per channel, and are supported by a 256K-Sample FIFO data buffer. Both continuous and burst clocking modes are supported, and voltage ranges are software-selectable as $\pm 10V$, $\pm 5V$ or $\pm 2.5V$. Clocking and triggering rates can be derived from an internal rate generator, or from external clock and trigger sources to support the synchronous operation of multiple boards.

Each analog output channel implements a weighted-DAC R-2R configuration, which minimizes latency and has no minimum clocking rate. The outputs can be software-configured either for single-ended operation or for 3-wire differential operation.

On-demand autocalibration determines and applies error correction for all output channels, and a selftest switching network permits board integrity to be verified by the host. Eight bidirectional digital I/O lines are programmable as inputs or outputs.

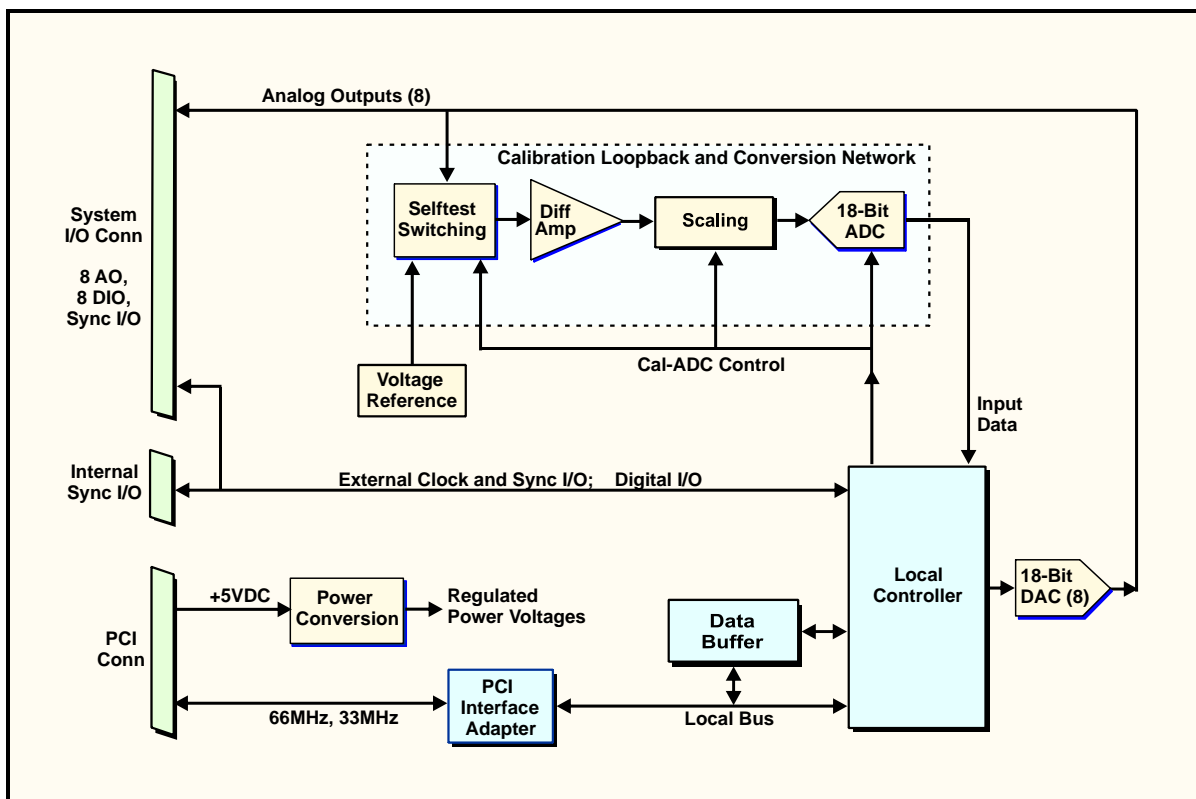


Figure 1. PMC66-18AO8; Functional Organization

This product complies with the IEEE PCI local bus specification Revision 2.3. System connections are made at the front panel through a high-density 68-Pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. Operation over the specified temperature range is achieved with conventional air cooling.

PERFORMANCE SPECIFICATIONS

At +25 °C, with specified operating voltages

Analog Output Characteristics:

Configuration:	Eight simultaneously clocked output channels with a dedicated 18-Bit R-2R DAC per channel. Software-selectable as either single-ended or 3-wire balanced differential. 4-Channel version also available.
Voltage Ranges:	±10V, ±5V or ±2.5V full scale for all output channels, software-selectable.
Output Resistance:	1.0 Ohm maximum at I/O connector pins.
Output protection:	Withstands sustained short-circuiting to ground
Loading:	Zero to ±3ma, any single channel. <i>Maximum total of 16mA on all outputs.</i> Stable with any load capacitance
Line Imbalance:	(Differential output mode) ±15mV max.
Signal/Noise Ratio (SNR):	90dB typical on ±10V range; 10Hz - 250kHz
Glitch Impulse:	12 nV-s, typical on ±5V range

Analog Output Transfer Characteristics:

Resolution:	18 Bits (0.0004 percent of FSR)		
Output Access:	256K-Sample FIFO buffer.		
DC Accuracy: (Max error, no-load)	<u>S.E. Range</u>	<u>S.E. Zero Accuracy</u>	<u>S.E. ±Fullscale Accuracy</u>
	±10V	±0.6mV	±1.7mV
	±5V	±0.4V	±1.2mV
	±2.5V	±0.3mV	±0.7mV
	<u>Diff Range*</u>	<u>Diff Zero Accuracy</u>	<u>Diff ±Fullscale Accuracy</u>
	±10V	±1.5mV	±6mV
	±5V	±1.2V	±4mV
	±2.5V	±1.0mV	±3mV
	* Differential output is measured between OUTPUT-XX-HI and OUTPUT-XX-LO.		
Settling Time:	6us to 0.1 percent of step, typical with halfscale step, no-load.		
Crosstalk Rejection:	90 dB minimum, DC-100 kHz		
Integral Nonlinearity:	±0.002 percent of FSR, maximum		
Differential Nonlinearity:	±0.001 percent of FSR, maximum		

Analog Output Operating Modes and Controls

Output Data Buffer:	256K-sample FIFO
Sample Clock Sources:	Internal rate generator; External Clock I/O, Software clock. 500kHz max.
Triggering Sources:	Internal rate generator, TTL external trigger I/O, Software trigger.
Clocking Modes:	Continuous or periodic. Supports triggered functions.
Internal Rate Generator:	Programmable from 3 to 500,000 output clocks per second. Divides Master Clock frequency to clocking rate using a 24-bit divider.
External Sync I/O:	Clock and trigger, selectable as TTL or LVDS.
Output Data Format:	18 Bits, selectable as offset binary or two's complement coding, with attached end-of-function flag and channel number.

Digital Input/Outputs:

Eight TTL I/O lines in two groups of four bits, group-configurable as inputs or outputs. 0.2ma maximum input loading as current source, 8ma output loading as either source or sink. Direct register control.

PCI Compatibility:

Conforms to PCI Specification 2.3, D32 read/write, 33/66MHz, universal (5V/3.3V) signaling, Supports block-mode DMA data transfers as bus master in two channels.

Power Requirements

+5VDC \pm 0.25 VDC at 1.3 Amps typical, 1.5 Amps maximum. Supplied by PCI bus.

PHYSICAL PARAMETERS

Physical Dimensions: (PMC Form Factor)

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side-1 is protected by an EMI shield.

Environmental Specifications

Ambient Temperature Range:	Operating	0 to +65 Degrees Celsius inlet air:
	Storage:	-40 to +85 Degrees Celsius
Relative Humidity:	Operating:	0 to 80%, non-condensing
	Storage:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.	
Cooling:	Conventional air cooling; 150 LFPM	

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C", as indicated below. For example, model number **PMC66-18AO8-8-40.32M** describes a PMC module with eight output channels and a 40.320MHz master clock frequency.

Basic Model Number	Form Factor
PMC66-18AO8	PMC (Native)
PCI66-18AO8¹	PCI, short length
Cpci66-18AO8¹	cPCI, 3U
PCle66-18AO8¹	cPCI, 3U
PC104P66-18AO8	PC104-Plus
PCle10466-18AO8^{1,2}	PCle, one-lane on PC/104 form factor

¹ Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

² PCle104 supports only the PCle bus.

Optional Parameter	Value	Specify Option As:
Number of Channels:	8 output channels	A = 8
	4 output channels	A = 4
Master Clock Frequency	Standard 40.32MHz.	C= 40.32M
	*	*
Custom Features	*	*

* Contact factory for custom frequencies, or for availability of other custom features..

SYSTEM INTERFACE CONNECTOR

Table 1. System I/O Connector

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	OUTPUT 00 LO	1	DIGITAL RTN
2	OUTPUT 00 HI	2	DIGIO 00
3	OUTPUT RTN 00	3	DIGITAL RTN
4	OUTPUT RTN 00	4	DIGIO 01
5	OUTPUT 01 LO	5	DIGITAL RTN
6	OUTPUT 01 HI	6	DIGIO 02
7	OUTPUT RTN 01	7	DIGITAL RTN
8	OUTPUT RTN 01	8	DIGIO 03
9	OUTPUT 02 LO	9	DIGITAL RTN
10	OUTPUT 02 HI	10	DIGIO 04
11	OUTPUT RTN 02	11	DIGITAL RTN
12	OUTPUT RTN 02	12	DIGIO 05
13	OUTPUT 03 LO	13	DIGITAL RTN
14	OUTPUT 03 HI	14	DIGIO 06
15	OUTPUT RTN 03	15	DIGITAL RTN
16	OUTPUT RTN 03	16	DIGIO 07
17	OUTPUT 04 LO	17	DIGITAL RTN
18	OUTPUT 04 HI	18	DIGITAL RTN
19	OUTPUT RTN 04	19	CLOCK INPUT LO *
20	OUTPUT RTN 04	20	CLOCK INPUT HI *
21	OUTPUT 05 LO	21	DIGITAL RTN
22	OUTPUT 05 HI	22	DIGITAL RTN
23	OUTPUT RTN 05	23	CLOCK OUTPUT LO *
24	OUTPUT RTN 05	24	CLOCK OUTPUT HI *
25	OUTPUT 06 LO	25	DIGITAL RTN
26	OUTPUT 06 HI	26	DIGITAL RTN
27	OUTPUT RTN 06	27	TRIGGER INPUT LO *
28	OUTPUT RTN 06	28	TRIGGER INPUT HI *
29	OUTPUT 07 LO	29	DIGITAL RTN
30	OUTPUT 07 HI	30	DIGITAL RTN
31	OUTPUT RTN 07	31	TRIGGER OUTPUT LO *
32	OUTPUT RTN 07	32	TRIGGER OUTPUT HI *
33	OUTPUT RTN 07	33	DIGITAL RTN
34	OUTPUT RTN 07	34	DIGITAL RTN

(All output returns "OUTPUT RTN XX" are connected together internally.)

Table 2. Sync-I/O Connector

PIN	SIGNAL
1	AUX CLOCK I/O LO *
2	AUX CLOCK I/O HI *
3	DIGITAL RTN
4	DIGITAL RTN
5	AUX TRIGGER I/O LO *
6	AUX TRIGGER I/O HI *

Recommended Sync-I/O mating cable connector is:
Molex# 51146-0600.

* (Table 1 and Table 2) Edge-detected LVDS or TTL. When TTL sync I/O is selected, 'HI' pins use TTL signal levels, and 'LO' pins are left disconnected. Software-selected assertion on LOW or HIGH transition.

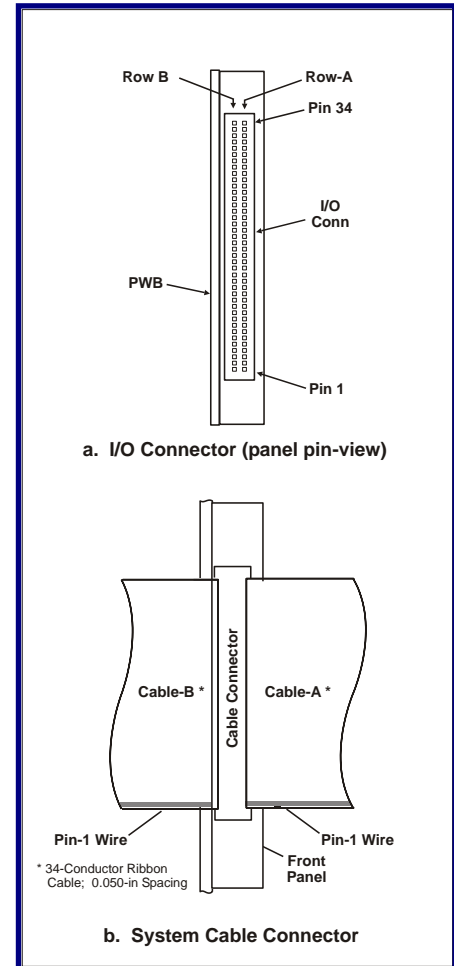


Figure 2. System I/O Connector

System Cable Mating Connector:

68-pin 0.050" Subminiature connector with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref):

Amp # 787170-7.

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