

# General Standards Corporation

High Performance Bus Interface Solutions

## 16AIO

### 16-Bit Analog Input/Output Board

*With 32 Input Channels, 4 Output Channels and 16-Bit Digital I/O Port*

Available in PMC, PCI, cPCI and PC104-Plus and PCI Express form factors as:

PMC-16AIO:	PMC, Single-width
PCI-16AIO:	PCI, short length
cPCI-16AIO:	cPCI, 3U
PC104P-16AIO:	PC104-Plus
PCIe-16AIO:	PCI Express
PCIe104-16AIO:	PCIe, one-lane on PC/104 form factor

See Ordering Information for details.

Call for the availability of other form factors, such as XMC, CCPMC, etc.

***This specification applies primarily to the PMC form-factor.***

#### **Features Include:**

- 32 Single-Ended or 16 Differential 16-Bit Scanned Analog Input Channels
- 4 Analog Output Channels, 16-Bit D/A Converter per Channel
- $\pm 15\text{mA}$  Peak Output Load Capacity Available
- 16-Bit Bi-directional Digital Port with Two Auxiliary I/O Lines
- Software-Selectable Analog Input/Output Ranges of  $\pm 10\text{V}$ ,  $\pm 5\text{V}$  or  $\pm 2.5\text{V}$ . Optional output ranges of 0 to  $+10\text{V}$ , 0 to  $+5\text{V}$ , 0 to  $+2.5\text{V}$ .
- Available also with 16 High-Level analog input channels, for monitoring high-level digital inputs.  $\pm 60\text{V}$ ,  $\pm 30\text{V}$ , or  $\pm 15\text{V}$ ; Configurable as 16 single-ended channels or 8 differential channels.
- Independent 32K-Sample Analog Input and Output FIFO Buffers
- 300K Samples per Second Aggregate Analog Input Sample Rate
- Multiple-Channel and Single-Channel Input Scanning Modes
- Low Crosstalk, Noise and Input Bias Current; Buffer Amplifiers on all Analog Input Lines
- 300K Samples per Second per Channel Analog Output Clocking Rate (1200 KSPS Aggregate Rate)
- Supports Waveform and Arbitrary Function Generation; Continuous and One-shot Modes
- Internal Rate Generator Controls Input Sampling, Output Sampling, or Both Simultaneously
- Supports Multiboard Synchronization of Analog Inputs and Outputs
- Internal Auto calibration of Analog Input and Output Channels
- Continuous and Burst (One-Shot) Input and Output Modes
- DMA Engine Minimizes Host I/O Overhead

#### **Applications:**

- Data Acquisition Systems
- Industrial Robotics
- Precision Voltage Sourcing and Measurement
- Automatic Test Equipment
- Function and Waveform Generation
- Research Instrumentation

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# ELECTRICAL SPECIFICATIONS

At +25 °C, with specified operating voltages

## ANALOG INPUT CHANNELS

### □ Input Characteristics:

Configuration:	32 input lines, configurable as 32 single-ended or 16 differential channels
Voltage Ranges:	Software configurable as $\pm 10$ , $\pm 5$ or $\pm 2.5$ Volts
Input Impedance:	1.0 Megohms line-to-ground, 2.0 Megohms line-to-line, in parallel with 100Pfd. Independent of scan rate. (180K $\pm$ 20K Line-to ground for High-Level inputs).
Bias Current:	80 nanoamps maximum
Signal to Noise (SNR):	80 dB typical
Common Mode Rejection:	60 dB typical, DC-60 Hz, differential input mode. (30dB for High-Level inputs).
Common Mode Range:	$\pm 10$ Volts; differential input configuration. ( $\pm 60$ Volts for High-Level inputs).
Overvoltage Protection:	Standard: $\pm 30$ Volts with power applied; $\pm 15$ Volts with power removed ( $\pm 70$ Volts for High-Level inputs).

### □ Transfer Characteristics:

Resolution:	16 Bits; 0.0015 percent of FSR
Maximum Conversion Rate:	300K conversions per second, minimum
Channels per scan:	2, 4, 8, 16, or 32 Channels per scan (32 channels available only in single-ended mode)
Maximum Scan Rate:	75K scans per second in multiple-channel mode. 150 KSPS in 2-Channel mode. 300KSPS in single-channel mode. Scan rate equals the conversion rate divided by the number of channels per scan.
Minimum Scan Rate:	400 scans per second, using a single internal rate generator; 0.007SPS using both generators. Zero, using a software sync flag or an externally supplied sync input.

DC Accuracy: (Maximum composite error, referred to inputs)	<u>Standard Inputs:</u>		
	<u>Range</u>	<u>Midscale Accuracy</u>	<u><math>\pm</math>Fullscale Accuracy</u>
	$\pm 10V$	$\pm 3.2mV$	$\pm 4.2mV$
	$\pm 5V$	$\pm 2.3mV$	$\pm 2.8mV$
	$\pm 2.5V$	$\pm 1.6mV$	$\pm 2.0mV$
	<u>High-Level Inputs:</u>		
	<u>Range</u>	<u>Midscale Accuracy</u>	<u><math>\pm</math>Fullscale Accuracy</u>
	$\pm 60V$	$\pm 30mV$	( $\pm 6\%$ of Range)
	$\pm 30V$	$\pm 17mV$	
	$\pm 15V$	$\pm 10mV$	

Crosstalk Rejection:	85dB, DC-10kHz
Integral Nonlinearity:	$\pm 0.003$ percent of FSR, maximum
Differential Nonlinearity:	$\pm 0.0015$ percent of FSR, maximum



## □ Analog Output Operating Modes and Controls

Clocking Modes:	<p>Simultaneous Continuous Mode: Channel values in a designated channel group are stored in an intermediate buffer, and then are transferred to the output DAC's when an output clock occurs. The clock can be generated either by the internal rate generator, by a software flag, or by an external hardware trigger. As many as three target boards can be clock-synchronized to a single initiator board.</p> <p>Simultaneous Burst Mode: A single function (i.e.: burst) is initiated by a software or hardware sync. During a burst, channel values in a designated channel group are stored in a transfer buffer, and then are transferred to the output DAC's each time a clock pulse is generated by the internal rate generator. The burst terminates when a Burst End flag is encountered</p> <p>Channel-Sequential Modes: Same as simultaneous modes, except each value in the data buffer is written immediately to the associated output DAC. The group-end flag is ignored in this mode.</p>
Channel Assignment:	A 2-bit field in the output buffer assigns the associated data field to a specific output channel.
Group End:	A single bit in the output buffer indicates the last value in a channel group.
Burst End:	A single bit in the output buffer indicates the last value in an output burst sequence.
Output Data Buffer:	32K-sample FIFO with 0000h-7FFEH adjustable threshold flag; DMA is supported

## **RATE GENERATORS**

Analog outputs and inputs can be clocked from either of two independent rate generators, or both inputs and outputs can be synchronized to a single generator. Each rate generator uses a 16-bit adjustable frequency divider, and the two generators can be operated in series to provide very low clocking rates.

## **DIGITAL I/O PORT**

The digital I/O port consists of 16 bidirectional data lines, one auxiliary input line and one auxiliary output line. An interrupt request can be generated in response to the auxiliary input. The data lines are organized as two data bytes, each of which can be configured independently as either an input or output byte. Standard TTL logic levels apply, with 8 ma source/sink capability per output line.

NOTE: For the PC104-Plus form-factor, the digital I/O port is only available with the –SCSI3 option.

## **PCI INTERFACE**

- **Compatibility:** Conforms to PCI Specification 2.3, with D32 read/write transactions.  
Supports "plug-n-play" initialization.  
Provides one multifunction interrupt.  
Supports DMA transfers as bus master.

# MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

## Power Requirements:

+5VDC  $\pm$ 0.2 VDC at 1.4 Amps, maximum, 0.9 Amps typical. (1.8 Amps maximum if all outputs are loaded to 15mA.)

## Mechanical Characteristics *(PMC form factor)*

Height: 13.5 mm (0.53 in)  
Depth: 143.75 mm (5.66 in)  
Width: 74.0 mm (2.91 in)

## Environmental Specifications

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius *
	Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius *
	Storage: -40 to +85 Degrees Celsius

\* Air temperature at board surface.

Relative Humidity: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.

Cooling: Conventional air cooling; 150 LFPM

## ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-AB-C-D-E", as indicated below. For example, model number PMC-16AIO-41-15MA-BP-SCSI3 describes a PMC module with four output channels, a bezel and EMI shield, 15MA bipolar analog outputs, and a SCSI-3 I/O connector

Basic Model Number	Form Factor
PMC-16AIO	PMC (Native)
PCI-16AIO <sup>1</sup>	PCI, short length
cPCI-16AIO <sup>1</sup>	cPCI, 3U
PCIe-16AIO <sup>1</sup>	PCI, short length
PC104P-16AIO	PC104-Plus (Native)
PCIe104-16AIO <sup>1,2</sup>	PCIe, one-lane on PC/104 form factor

<sup>1</sup> Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

<sup>2</sup> PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Analog Outputs	No Output Channels	A = 0
	4 Output Channels	A = 4
EMI Shield (Now standard)	No bezel or shield	B = 0
	Bezel & shield installed	B = 1
Custom Features	No Custom Features	C = 0
	16 High-Level $\pm 60V$ analog input channels	C = 16HV60V
	High-current analog outputs; $\pm 15mA$ <sup>1</sup>	C = 15MA
Software-Selectable Output Ranges	Bipolar: $\pm 10V$ , $\pm 5V$ , $\pm 2.5V$	D = BP
	Unipolar: 0 to $+10V$ , 0 to $+5V$ , 0 to $+2.5V$	D = UP
System I/O Connector	Robinson Nugent 68-Pin IDC <sup>2</sup>	E = 0 <sup>2</sup>
	AMP 68-Pin SCSI-3	E = SCSI3

<sup>1</sup> Zero to  $\pm 15$  peak-mA per output channel; 40 mA-RMS maximum total loading for all four outputs. If all outputs are loaded to 15mA, power consumption may exceed the maximum level recommended for PMC modules.

<sup>2</sup> Native PMC form factor. Not currently available for PC104P. The PC104P form factor is available with either a standard 50-pin I/O connector or optionally, a SCSI-3 connector. The digital I/O signals are not available with the 50-pin connector version.

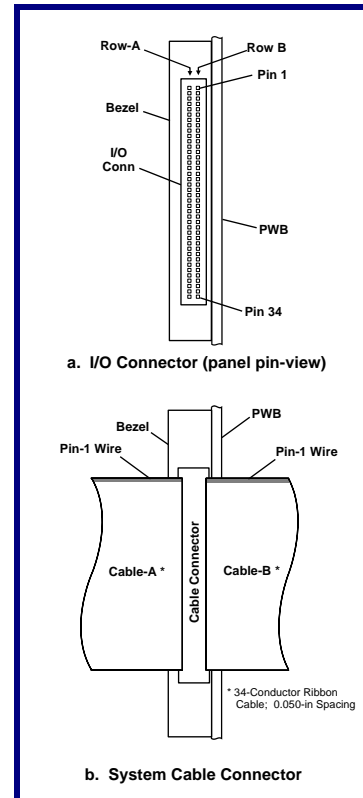
# SYSTEM I/O CONNECTIONS

**Table 1. System Connector Pin Functions**

ROW-A		ROW-B	
PIN	SIGNAL *	PIN	SIGNAL
34	ANA INP00 HI	34	ANA OUT00
33	ANA INP00 LO **	33	OUTPUT RTN
32	ANA INP02 HI	32	ANA OUT01
31	ANA INP02 LO	31	OUTPUT RTN
30	ANA INP04 HI	30	ANA OUT02
29	ANA INP04 LO	29	OUTPUT RTN
28	ANA INP06 HI	28	ANA OUT03
27	ANA INP06 LO	27	OUTPUT RTN
26	ANA INP08 HI	26	VTEST
25	ANA INP08 LO	25	VTEST RTN
24	ANA INP10 HI	24	DIGITAL RTN
23	ANA INP10 LO	23	AUX DIGITAL IN
22	ANA INP12 HI	22	AUX DIGITAL OUT
21	ANA INP12 LO	21	DIG IO 00
20	ANA INP14 HI	20	DIG IO 01
19	ANA INP14 LO	19	DIG IO 02
18	INPUT RTN	18	DIG IO 03
17	INPUT RTN	17	DIG IO 04
16	ANA INP16 HI	16	DIG IO 05
15	ANA INP16 LO	15	DIG IO 06
14	ANA INP18 HI	14	DIG IO 07
13	ANA INP18 LO	13	DIG IO 08
12	ANA INP20 HI	12	DIG IO 09
11	ANA INP20 LO	11	DIG IO 10
10	ANA INP22 HI	10	DIG IO 11
9	ANA INP22 LO	9	DIG IO 12
8	ANA INP24 HI	8	DIG IO 13
7	ANA INP24 LO	7	DIG IO 14
6	ANA INP26 HI	6	DIG IO 15
5	ANA INP26 LO	5	DIGITAL RTN
4	ANA INP28 HI	4	SYNC OUTPUT
3	ANA INP28 LO	3	DIGITAL RTN
2	ANA INP30 HI	2	SYNC INPUT
1	ANA INP30 LO	1	DIGITAL RTN

\* Input channels 16-30 (Single-ended 16-31) can be supplied with optional high-level input ranges of  $\pm 60V$ , 30V, 15V. See ordering options.

\*\* Analog inputs are shown for the differential input mode. In single-ended mode, LO inputs become consecutive odd-numbered channels, beginning with ANA INP 01 replacing ANA INP 00 LO, etc.



**Figure 2. System Input/Output Connector**

**System Mating Connector:**

**Robinson-Nugent Option:**

68-Pin 2-row 0.050" dual-ribbon cable socket connector:  
Robinson Nugent #P50E-068-S-TG,  
or equivalent.

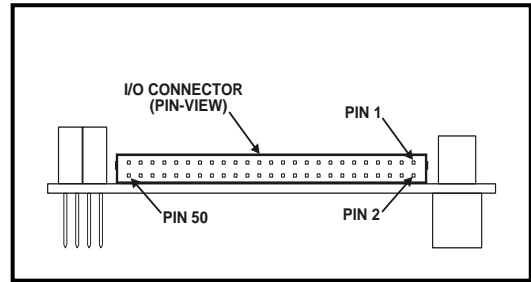
**SCSI3 Option:**

68-pin 0.050" Subminiature connector with metal shield:  
AMP #749621-7 or equivalent.

**Table 2. System Connector Pin Functions for the PC104P 50-Pin Connector**

PIN	FUNCTION	PIN	FUNCTION
1	INPUT RTN	26	ANA INP 22 LO
2	INPUT RTN	27	ANA INP 24 HI
3	ANA INP 00 HI	28	ANA INP 24 LO
4	ANA INP 00 LO	29	ANA INP 26 HI
5	ANA INP 02 HI	30	ANA INP 26 LO
6	ANA INP 02 LO	31	ANA INP 28 HI
7	ANA INP 04 HI	32	ANA INP 28 LO
8	ANA INP 04 LO	33	ANA INP 30 HI
9	ANA INP 06 HI	34	ANA INP 30 LO
10	ANA INP 06 LO	35	ANA OUT 03
11	ANA INP 08 HI	36	ANA OUT 02
12	ANA INP 08 LO	37	ANA OUT 01
13	ANA INP 10 HI	38	ANA OUT 00
14	ANA INP 10 LO	39	VTEST
15	ANA INP 12 HI	40	OUTPUT RTN
16	ANA INP 12 LO	41	TRIG OUT
17	ANA INP 14 HI	42	N/C
18	ANA INP 14 LO	43	N/C
19	ANA INP 16 HI	44	N/C
20	ANA INP 16 LO	45	TRIG IN
21	ANA INP 18 HI	46	N/C
22	ANA INP 18 LO	47	VTEST RTN
23	ANA INP 20 HI	48	N/C
24	ANA INP 20 LO	49	+5VDC
25	ANA INP 22 HI	50	DIGITAL RTN

\* Analog inputs are shown for the differential input mode. In single-ended mode, LO inputs become consecutive odd-numbered channels, beginning with ANA INP 01 replacing ANA INP 00 LO.



**Figure 2. System Input/Output Connector**

**System Mating Connector:**  
**Polarized 50-Pin socket connector:**  
**AMP #1-746288-0,**  
**with strain-relief #499252-4.**

**General Standards Corp.**

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