

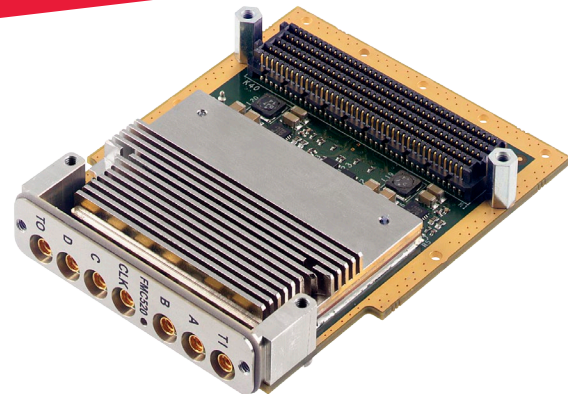


# FMC-520

4-channel 1 GSPS, 2x to 4x Interpolating, 16-bit Analog Output FMC

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### Applications

- ◆ Software Radio
- ◆ Electronic Counter Measures (ECM)
- ◆ Radar
- ◆ Broadband Wireless Access (BWA)
- ◆ WiMAX 802.16

### Features

- ◆ Four analog output channels updating from FPGA at 500 MSPS or
- ◆ Two analog output channels updating from FPGA at 1.0 GSPS
- ◆ 775 MHz output bandwidth
- ◆ Onboard or external sample clock
- ◆ FMC/VITA 57 form factor
- ◆ Air- or conduction-cooled rugged versions

### Benefits

- ◆ Direct DAC connection to host FPGA ensures maximum throughput
- ◆ Able to synchronize multiple channels/boards
- ◆ Easily interfaces to FPGA-based host board
- ◆ Complete DAC I/O

### Overview

The FMC-520 is a 4-channel 1000 MSPS analog output FPGA Mezzanine Card (FMC) based on the VITA 57 specification. This specification allows I/O devices to be directly coupled to a host FPGA. On the FMC-520, the two dual-channel DAC devices connect through the high-bandwidth FMC connector to an FPGA-based host board which maximizes data throughput and minimizes latency.

The FMC-520 can be used on platforms like Curtiss-Wright Controls Embedded Computing's (CWCEC) FPE320, FPE650, and HPE720 which all provide Xilinx® Virtex®-5 FPGA processor nodes.

### Analog Output

The FMC-520 supports four analog outputs through MMCX type front panel connectors. The analog outputs are 50 Ω single-ended, transformer coupled. The analog signal paths of both DAC outputs are matched to within 4 ps to allow synchronous operation of the DACs. The "full scale" analog output voltage is 1.0 Vpp.

### Clocking

The onboard programmable VCXO has a range of frequencies from:

- ◆ 10 MHz to 945 MHz
- ◆ 970 MHz to 1134 MHz
- ◆ 1213 MHz to 1417.5 MHz.

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This clock can be locked to an external 10 MHz reference provided through the external clock input connector. The FMC can provide an output signal from the clock circuit, multiplexed onto the TRIG OUT connector and also supports external full rate update clock.

The external front panel clock input is through a MMCX type front panel connector. It is single-ended, 50 Ω AC coupled, LVPECL. The FMC-520 is capable of synchronous operation, phase aligned with other FMC-520 boards, when using the external clock source.

### Triggering

Trigger In and Trigger Out MMCX type front panel connectors. Actual functionality of these signals is dependent on the HDL code in the FPGA of the host carrier card.

Trigger In is a single-ended 50 Ω (Thevenin) LVPECL input signal. Trigger Out is a single-ended LVPECL output signal capable of driving a 50 Ω (Thevenin) termination. This line may be multiplexed with the clock output.

It is possible to synchronize the DACs on multiple FMC-520's using the Trigger In and Trigger Out signals. The FMC-520 FusionXF Hardware Development Kit (HDK) and Software Development Kit (SDK) support this functionality.

### Digital to Analog Converter

Each of the two TI DAC5682Z devices used on the FMC-520 is a 16-bit, 1000 MSPS digital to analog converter with a 16-bit wideband LVDS data bus from the FMC-520's host FPGA. Full rate input data can be transferred to a single DAC channel. Alternatively, interleaved half-rate or quarter-rate input data can be interpolated by internal 2x or 4x FIR filters to both channels. Each interpolation FIR is configurable in either Low-Pass or High-Pass mode, allowing the selection of a higher order output spectral image.

Each DAC allows both complex or real output. The DAC5682Z can receive an interleaved complex I/Q baseband input data stream through the LVDS port and increase the sample rate through interpolation by a factor of two or four.

The HDL and software of the FMC-520 support two main operating modes for each device: two channels with a 500 MSPS update rate from the FPGA or a single channel with a 1 GSPS update rate.

### FusionXF Software/HDL Support

CWCEC's FusionXF development kit includes software, HDL and utilities with examples and infrastructure for using the FMC-520 on each supported host.

One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA. It facilitates the inclusion of signal processing blocks such as digital up converters, making HDL development easier and integration more straightforward.

Table 1: Specifications

Analog Output	
Number of Channels	4
Update Rate	Up to 1.0 GSPS
Full Scale Output Voltage	1 Vpp (adjustable via register settings)
Device	2x TI DAC5682Z
Output Bandwidth (3 dB)	775 MHz
Output Impedance	50 Ohm, AC coupled
Output Connector	Front panel MMCX
SNR (device)	70 dBc <sup>1</sup>
SFDR (device)	80 dBc <sup>2</sup>
IMD3 (device)	88 dBc <sup>3</sup>
ACLR (device)	83 dBc <sup>4</sup>
Clock & Trigger Inputs	
Clock Input Connector	Front panel MMCX
Clock Input	50 Ohm, AC coupled LVPECL
Clock Input Frequency	up to 1 GHz
Trigger Input/Output	Single-ended, 50 Ohm, LVPECL buffered to host FPGA
Software/HDL	
Host HDL Code	Analog output hosted by FusionXF on FPE650 6U quad FPGA VPX (contact CWCEC for other hosts)
Misc.	
I2C bus	Atmel AT24C512B Serial EEPROM; AD7414 to monitor DAC temp
Environmental	
Ruggedization Levels	Air-cooled Air-cooled Rugged Conduction-cooled

Notes

1. CLKIN = 1000 MHz, DACA + DACB on, single tone, 0dBFS, IF = 20.1 MHz
2. CLKIN = 1000 MHz, DACA + DACB on, first Nyquist zone <  $f_{data}/2$ , IF = 5.1 MHz
3. 3rd order 2-tone inter-modulation; CLKIN = 1000 MHz, DACA + DACB on, IF = 20.1 MHz and 21.1 MHz
4. Adjacent channel leakage ratio; CLKIN = 983 MHz, DACA + DACB on, single carrier, baseband.



Table 2: Specifications

Part number extension		Air-Cooled			Conduction-Cooled	
		Level 0	Level 100	Level 200 (Note 6)	Level 100	Level 200 (Note 6)
Temperature	Operational (Air-Cooled Note 4) (Conduction-Cooled Note 7)	0°C to +50°C	-40°C to +71°C	-40°C to +85°C	-40°C to +71°C	-40°C to +85°C
	Non-operational (storage)	-40°C to +85°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Vibration	Sine (Note 1)	2 g peak 15-2 k Hz	10 g peak 15-2 k Hz	10 g peak 15-2 k Hz	10 g peak 15-2 k Hz	10 g peak 15-2 k Hz
	Random (Note 2)	0.01 g2/Hz 15-2 k Hz	0.04 g2/Hz 15-2 k Hz	0.04 g2/Hz 15-2 k Hz	0.1 g2/Hz 15-2 k Hz	0.1 g2/Hz 15-2 k Hz
Shock (Note 3)	Operational	20 g peak	30 g peak	30 g peak	40 g peak	40 g peak
Humidity	Operational	0-95% non-condensing	0-100% non-condensing	0-100% non-condensing	0-100% non-condensing	0-100% non-condensing
	Non-operational (storage)	0-95% non-condensing	0-100% condensing	0-100% condensing	0-100% condensing	0-100% condensing
Conformal Coat (Note 5)		No	Yes	Yes	Yes	Yes
2 Level Maintenance Ready		-	-	-	No	No

Notes:

1. Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15 to 44 Hz, depending on specific test equipment.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Standard air-flow is 8 cfm at sea level. Some higher-powered products may require additional airflow. Consult the factory for details.
5. Conformal coating type is manufacturing site specific. Consult the factory for details.
6. This is a non-standard product. Consult factory for availability.
7. Temperature is measured at the card edge.

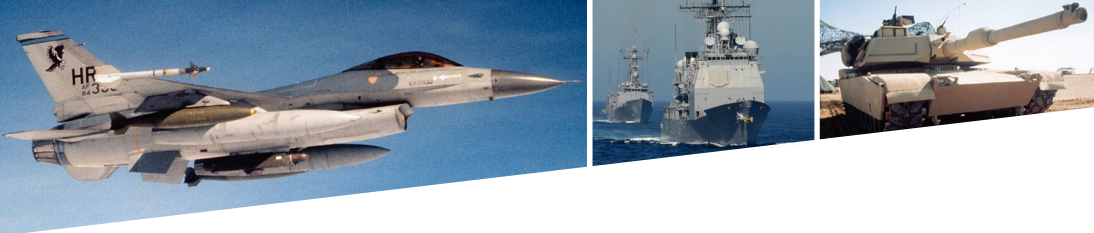
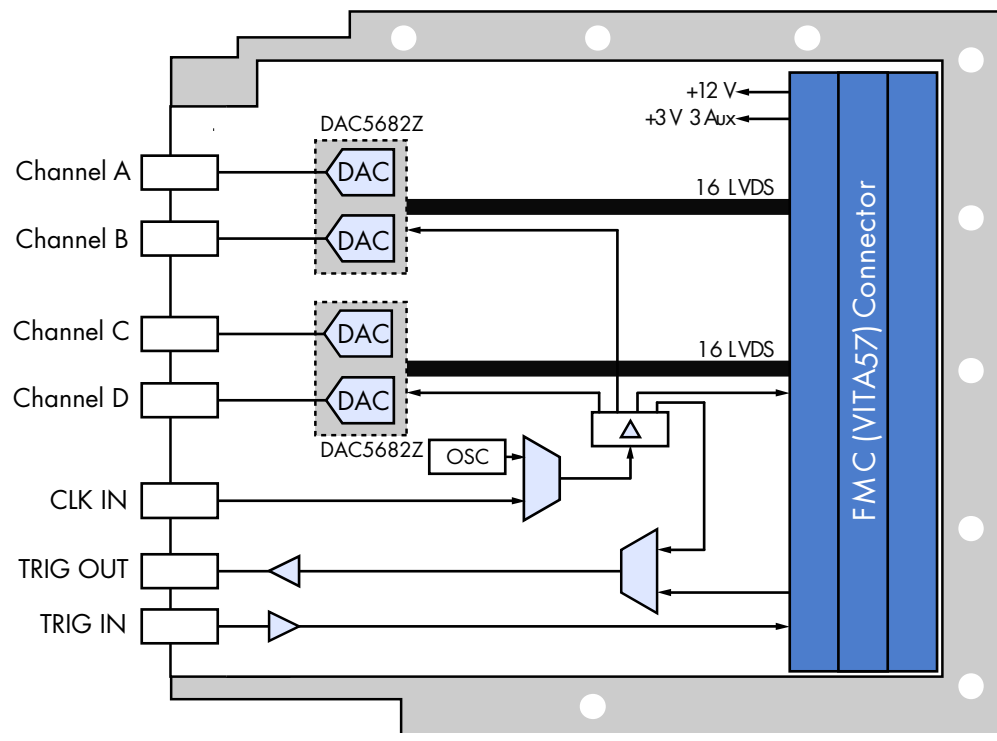


Figure 1: FMC520 Block Diagram



**Warranty**

This product has a one year warranty.

**Contact Information**

To find your appropriate sales representative, please visit:

Website: [www.cwembedded.com/sales](http://www.cwembedded.com/sales)

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