



Real Time, High Performance Acquisition Solutions



Overview

The ADF-Q55 sets a new benchmark for high speed, high performance analog-digital conversion products. By compressing 4 TI 550Msps analog-digital converters into an FMC form factor, DEG engineers have created the industry's highest density high-speed FMC product in the embedded marketplace. This FPGA mezzanine card (FMC) converts four channels of up to 2.3GHz analog input bandwidth at 550Msps and 12-bit resolution. Based on the VITA 57 specification, the ADF-Q55 enables direct coupling of unparalleled analog-digital conversion capability with the VME/VXS/AMC/VPX/PCI-E carrier board of your choice. DEG engineers have designed this product and associated HDL firmware to work with both Altera and Xilinx FPGA's.

The ADF-Q55 is based on the Texas Instrument ADS54RF63 analog-digital converter and the emerging FMC form factor. DEG engineers leveraged design work and intellectual property from the highly successful ADC-3595 PMC board to bring ADF-Q55 to market in record time. By coupling this core architecture with the compact and flexible FMC form factor, DEG has enabled customers to rapidly and cost-effectively build compact & rugged systems with 4-8 channels of high-speed digitization on a single high performance processor/carrier board. This flexible approach reduces overall power consumption, footprint, and cost while increasing ruggedness and reliability.

Features

- Four 550Msps, 12-bit ADC's
- 2.3GHz Input Bandwidth
- FMC/VITA 57 Form Factor
- Air and Conduction-Cooled

Benefits

- Extremely Dense Digitization
- Works with Altera & Xilinx FPGA's
- Industry Standard Form Factor
- Rugged and Reliable

Performance

- 40Msps to 550Msps sampling rate
- Up to 2.3GHz Input Bandwidth
- ENOB = 9.9 Effective Bits, $F_{IN} = 550\text{MHz}$
- 8 Channels in Single VXS/VPX Slot



ADF-Q55 Details

The front panel of the ADF-Q55 has a μ -connector CMM220 that provides seven 50Ω inputs and one digital port. The digital port provides 4 LVDS pairs for general purpose use. The ADF-Q55 can be clocked by either external clocks, internal reference, external reference, or carrier board reference. With external clocks, the ADF-Q55 can be split into two pairs of ADC's with each pair driven by separate clocks or all four ADC's driven by one clock.

Analog Input

The Analog Input is single-ended with a full-scale input of 1.56VPP. The Analog Input signal bandwidth extends up to 2.3GHz. Customizable attenuation may be available for select customers. Maximum input is 7dBm.

Clocks & Triggers

The user can provide a clock input signal or use the onboard PLL to provide the board's clock. The clock input design accommodates a typical frequency of 550MHz but may operate at clock frequencies between 40MHz and 550MHz.

The various PLL options can be locked to an external 10MHz reference provided through the external clock input connector. PLL reference input must be a sine wave or square wave, with an amplitude range of 2dBm to +10dBm at 10MHz, with a 50 duty cycle. Different PLL frequencies can be accommodated prior to customer shipment.

Trigger input must be an 800MV to 3.3V peak-to-peak signal with a rise time of less than 10 nanoseconds. A trigger event is initiated by a positive transition on the trigger input. At the end of a capture event, the trigger circuitry is reset to wait for another trigger event. An auto-trigger function enables signal capture without an external trigger.

ADCLink

FMC modules are distinct and separate from the FPGA devices that support them. Initiation and control of the ADF-Q55 is accomplished with ADCLink. Board support packages are required for each unique host card.

The capabilities of ADCLink include, clock phase adjustment, onboard/external reference clock control, trigger input delays and thresholds, sampling delay adjustments and variable ADC gain.

ADF-Q55 Performance Specifications

Analog Specification	
Number of Channels	4
Sampling Rate	40Msps - 550Msps
Input Bandwidth	Up to 2.3GHz
Input Impedance	50Ω , AC coupled
Full Scale Input	Single-Ended, 1.56Vpp
Maximum Input	7dBm
SNR	61.9dBc @ $F_{IN} = 450\text{MHz}$
SFDR	-75dBc @ $F_{IN} = 450\text{MHz}$
ENOB	9.9 Effective bits @ $F_{IN} = 550\text{MHz}$

Clock & Trigger Specifications	
Connectors	μ -connector CMM 220
Clock Input	50Ω , AC coupled
Clock Input Frequency	40MHz to 550MHz
Internal Clock	10MHz
Std PLL Frequencies	Multiple, 150 - 550MHz
Trigger Input	Single-ended, 50Ω



Delphi Engineering Group, Inc.
www.delphieng.com

UNITRONIX Pty Ltd

PO Box 486, Morisset NSW 2264

NSW: Tel: 61 2 4977 3511 Fax: 61 2 4977 3522

WA: Tel: 61 8 9455 2424 Fax: 61 8 9455 2458

unitsyd@unitronix.com.au www.unitronix.com.au



Product Selection Guide

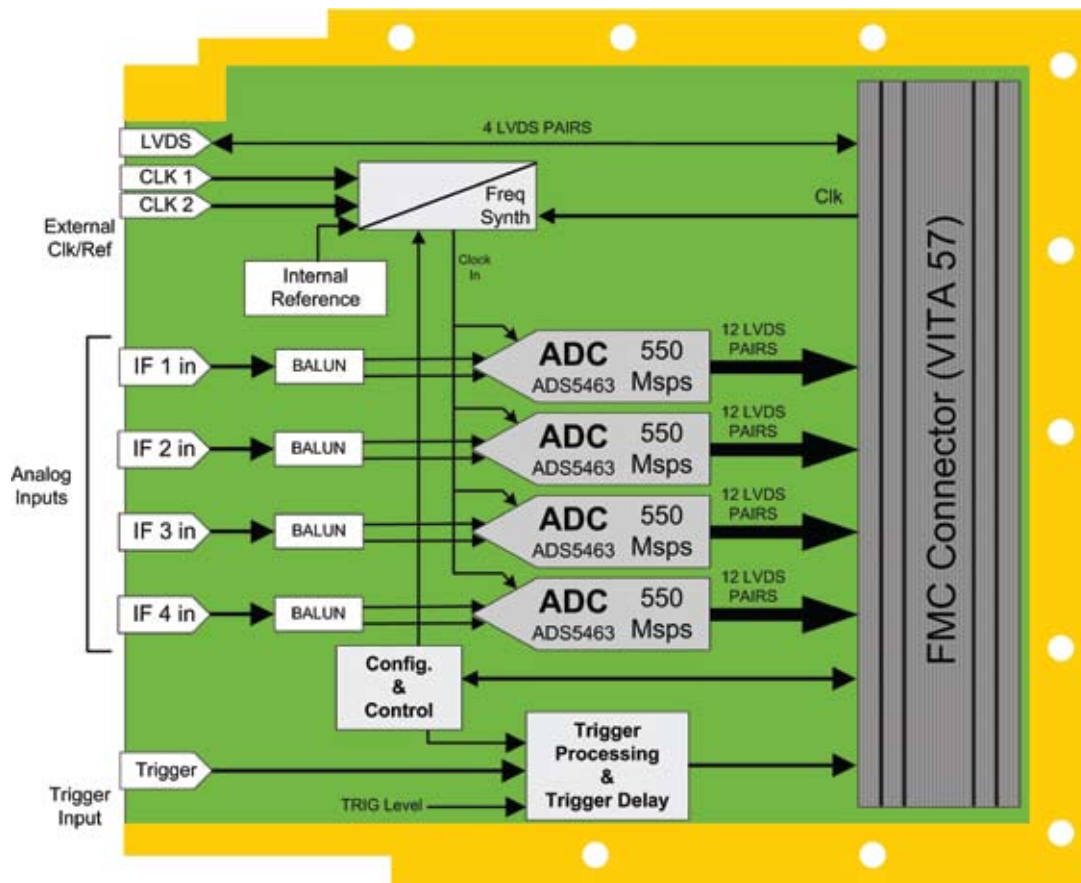
Part Number	Coupling	Rugged Level	Commercial	Rugged	Conduction Cooled	Conformal Coated
ADF-Q55	AC	Commercial	√	-	-	-
ADF-Q55-C	AC	Commercial	√	-	-	√
ADF-Q55-R	AC	Rugged	-	√	-	-
ADF-Q55-RC	AC	Rugged	-	√	-	√
ADF-Q55-CC	AC	Conduction	-	-	√	-
ADF-Q55-CCC	AC	Conduction	-	-	√	√

ADF-Q55 Environmentals

Environmental Specifications	Commercial	Rugged	Conduction Cooled
Operating Temperature	0°C to +50°C (inlet air)	-40°C to +71°C (inlet air)	-40°C to +71°C (inlet air)
Storage Temperature	-55°C to +85°C	-55°C to +125°C	-55°C to +125°C
Humidity (non-condensing)	0 to 95%	0 to 100%	0 to 100%
Vibration (Random)	0.01g ² /Hz 15-2,000Hz	0.04g ² /Hz 15-2,000Hz	0.1g ² /Hz 15-2,000Hz
Shock	20g peak	30g peak	40g peak

Notes: Based on Mil-Spec 810F

ADX-Q55 Block Diagram



For more information or details, please contact:



485 East 17th Street, Ste. 400
Costa Mesa, CA 92627
www.delphieng.com

Telephone: (949)515-1490
Fax: (949)515-1491
Email: sales@delphieng.com