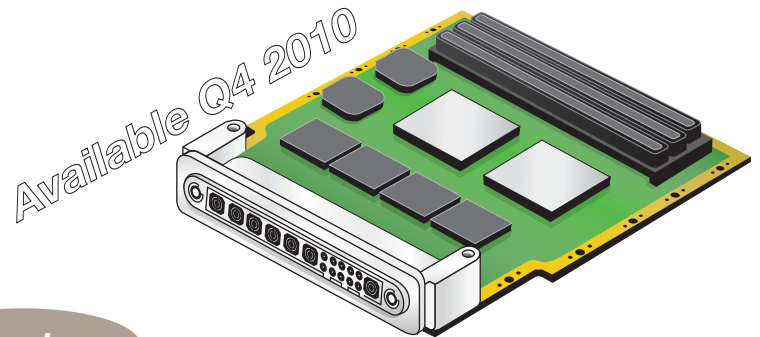




Real Time, High Performance Acquisition Solutions



Overview

The ADF-QSIG sets a new benchmark for high-speed, high resolution analog-digital conversion products. By compressing four industry-leading analog-digital converters in the FMC form factor, DEG engineers have created the highest density SIGINT FMC product in the marketplace. This FPGA Mezzanine Card (FMC) converts four channels of up to 750 MHz analog input bandwidth at 260Msps and 16-bit resolution. Based on the VITA 57 specification, the ADF-QSIG enables direct coupling of unparalleled analog-digital conversion capability with the VME/VXS/AMC/VPX/PCI-E carrier board of your choice. DEG engineers have designed this product and associated HDL firmware to work with both Altera and Xilinx FPGAs.

The ADF-QSIG is based on the the newest and most innovative analog-digital converter product line soon to be released. DEG engineers are leveraging design work and intellectual property from the highly successful ADF-Q40/55 product line to ensure customer access to this technology in record time. By coupling this core architecture with the compact and flexible FMC form factor, DEG has enabled customers to build cost-effective compact and rugged systems with 4-8 channels of high-speed with 4-8 channels of high-speed digitization in a single high performance processor/carrier board. This flexible approach reduces overall power consumption footprint, and cost while increasing ruggedness and reliability.

Features

- Four 260Msps, 16-bit ADC's
- 750MHz Input Bandwidth
- FMC/VITA 57 Form Factor
- Air and Conduction-Cooled

Benefits

- Extremely Dense Digitization
- Works with Altera & Xilinx FPGA's
- Industry Standard Form Factor
- Rugged and Reliable

Performance

- 10Msps to 260Msps sampling rate
- Up to 750MHz Input Bandwidth
- ENOB = 13 Effective Bits, $F_{IN} = 250\text{MHz}$
- 8 Channels in Single VXS/VPX Slot



ADF-QSIG Details

The front panel of the ADF-QSIG has amicro-connector CMM 220 and an HDMI connector. The micro-connector supports six 50Ω connections. A breakout cable converts the micro-connector ports to male SMA connectors. These connectors provide the ports for analog source, clock input, external reference clock, and trigger input. The HDMI connector supports the four pairs of front panel LVDS.

Analog Input

The Analog Input is single-ended with a full-scale input of 2.25VPP. The Analog Input signal bandwidth extends up to 750MHz. Customizable attenuation may be available for select customers. Maximum input is 10dBm.

Clocks & Triggers

The user can provide a clock input signal or use the onboard PLL to provide the board's clock. The clock input design accomodates a typical frequency of 250MHz but may operate at clock frequencies between 10MHz and 260MHz.

The various PLL options can be locked to an external 10MHz reference provided through the external clock input connector. PLL reference input must be a sine wave or square wave, with an amplitude range of 2dBm to +10dBm at 10MHz, with a 50 duty cycle. Different PLL frequencies can be accommodated prior to customer shipment.

Trigger input must be an 800MV to 3.3V peak-to-peak signal with a rise time of less than 10 nanoseconds. A trigger event is initiated by a positive transition on the trigger input. At the end of a capture event, the trigger circuitry is reset to wait for another trigger event. An auto-trigger function enables signal capture without an external trigger.

ADCLink

FMC modules are distinct and separate from the FPGA devices that support them. Initiation and control of the ADF-QSIG is accomplished with ADCLink. Board support packages are required for each unique host card.

The capabilities of ADCLink include, clock phase adjustment, onboard/external reference clock control, trigger input delays and thresholds, sampling delay adjustments and variable ADC gain.

ADF-QSIG Performance Specifications

Analog Specification	
Number of Channels	4
Available ADC Devices	10, 25, 65,105,170,210, 260 Msps
Sampling Rate	10Msps - 260Msps
Input Bandwidth	Up to 750MHz
Input Impedance	50Ω, AC coupled
Full Scale Input	Single-Ended, 2.25Vpp
Maximum Input	10dBm
SNR	79dBc @ $F_{IN} = 250\text{MHz}$
SFDR	-110dBc @ $F_{IN} = 25\text{MHz}$ -90dBc @ $F_{IN} = 250\text{MHz}$
ENOB	13 Effective bits @ $F_{IN} = 250\text{MHz}$

Clock & Trigger Specifications	
Connectors	μ-connector CMM 220
Clock Input	50Ω, AC coupled
Clock Input Frequency	10Mhz - 260Mhz
Internal Clock	10Mhz
Trigger Input	Single-ended, 50Ω



Product Selection Guide

Part Number	Coupling	Rugged Level	Commercial	Rugged	Conduction Cooled	Conformal Coated
ADF-Q260	AC	Commercial	√	-	-	-
ADF-Q260-C	AC	Commercial	√	-	-	√
ADF-Q260-R	AC	Rugged	-	√	-	-
ADF-Q260-RC	AC	Rugged	-	√	-	√
ADF-Q260-CC	AC	Conduction	-	-	√	-
ADF-Q260-CCC	AC	Conduction	-	-	√	√

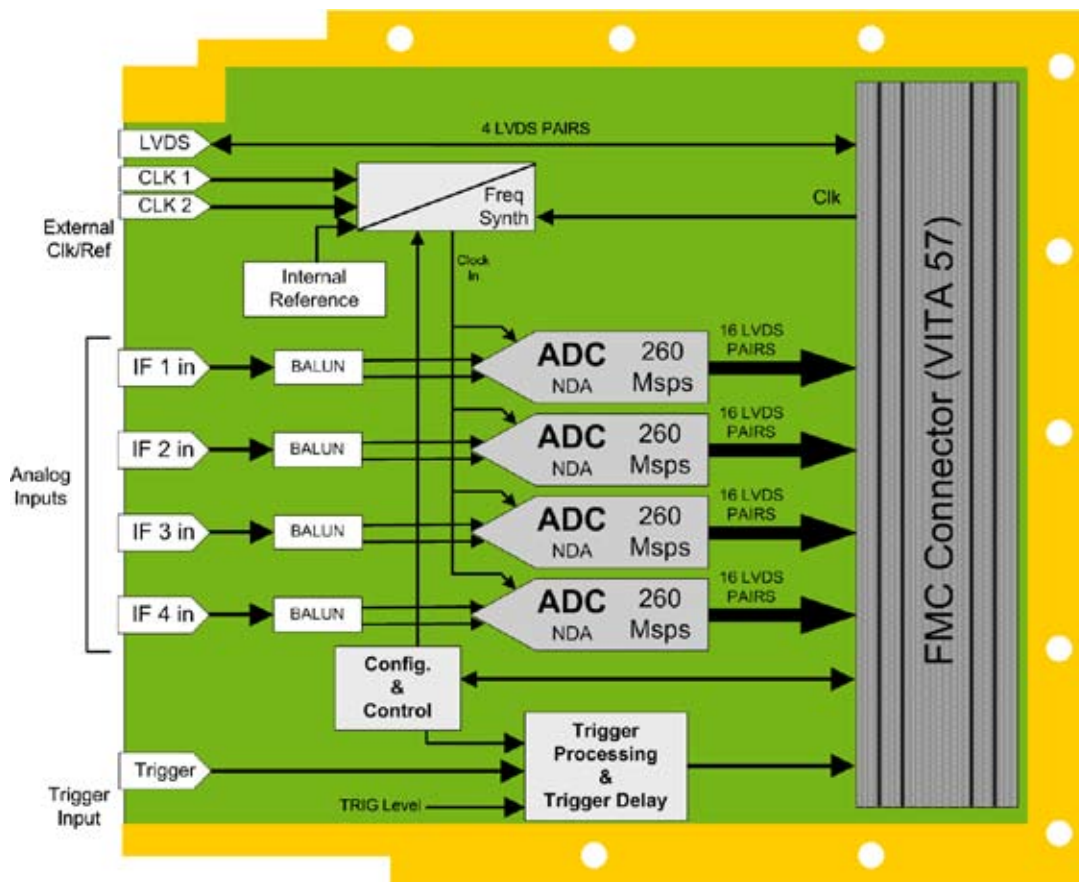
For different maximum sampling rates, substitute speed choice in part number. Example: for a 105Msps ADC, part becomes ADF-Q105

ADF-QSIG Environmentals

Environmental Specifications	Commercial	Rugged	Conduction Cooled
Operating Temperature	0°C to +50°C (inlet air)	-40°C to +71°C (inlet air)	-40°C to +71°C (inlet air)
Storage Temperature	-55°C to +85°C	-55°C to +125°C	-55°C to +125°C
Humidity (non-condensing)	0 to 95%	0 to 100%	0 to 100%
Vibration (Random)	0.01g ² /Hz 15-2,000Hz	0.04g ² /Hz 15-2,000Hz	0.1g ² /Hz 15-2,000Hz
Shock	20g peak	30g peak	40g peak

Notes: Based on Mil-Spec 810F

ADF-QSIG Block Diagram



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