

# General Standards Corporation

High Performance Bus Interface Solutions

## 66-16HSDI4AO4

16-Bit, 8-Channel, 1-MSPS PMC Analog Input/Output Board

With Four Simultaneously Sampled Sigma-Delta Analog Inputs,  
and Four Buffered Analog Outputs,

Available in PMC, PCI, cPCI and PC104-Plus and PCI Express form factors as:

<b>PMC66-16HSDI4AO4:</b>	<b>PMC</b> , Single-width
<b>PCI66-16HSDI4AO4:</b>	<b>PCI</b> , short length
<b>Cpci66-16HSDI4AO4:</b>	<b>cPCI</b> , 3U
<b>PC104P66-16HSDI4AO4:</b>	<b>PC104-Plus</b>
<b>PCle66-16HSDI4AO4:</b>	<b>PCI Express</b>
<b>PCle10466-16HSDI4AO4:</b>	<b>PCle</b> , one-lane on PC/104 form factor

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See Ordering Information for details.

Call for availability of other form factors, such as XMC, CCPMC, etc.

### FEATURES:

- **Analog Inputs:**
  - Four Differential Sigma-Delta Analog Inputs with Dedicated 16-Bit ADC per Channel
  - Simultaneous Sigma-Delta Sampling of all Inputs to 1.0 MSPS per channel
  - Sigma-Delta A/D Architecture; Minimal or no antialiasing requirements
- **Analog Outputs:**
  - 4 Single-Ended Analog Outputs with Dedicated 16-Bit DAC per Channel
  - Simultaneous Output Clocking Rates from 30 KSPS to 1.0 MSPS per Channel
  - Selectable Direct-Write or FIFO-Buffered Access
  - Buffer Configurable as Open for Data Streaming, or Circular for Periodic Functions
- **Common Analog I/O Features:**
  - Independent Input and Output Ranges:  $\pm 10V$ ,  $\pm 5V$ ,  $\pm 2.5V$
  - Independent 256-Ksample Input and Output FIFO Data Buffers
  - Hardware Clock and Sync I/O for Multiboard Operation
  - Output Clocking can be Synchronized with Input Sampling
  - Optional software-controlled master clock frequency deviation
  - Internal Power Conversion; Single 5-Volt Power Requirement
  - DMA Engine Supports Block-Mode and Demand-Mode Bus Transactions
  - Timing Controlled by Internal Rate Generator, by Software Clocking, or Externally
  - Internal On-Demand Autocalibration
- 16-Bit Bidirectional TTL Digital I/O Port
- 66 MHz 32-Bit PCI Support, with Universal 5V/3.3V Signaling
- Single-Width PMC Form Factor with Integral EMI Shield
- I/O Connector Pin-Compatible with PMC66-16AISS8AO4 for Four Input Channels

### TYPICAL APPLICATIONS:

- ✓ High Performance Data Acquisition
- ✓ Event Capture
- ✓ Robotics
- ✓ Arbitrary Waveform Generation
- ✓ Ultrasound
- ✓ Positioning Systems

REV: 081510

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## FUNCTIONAL DESCRIPTION

The 16-Bit PMC-16HSDI4AO4 analog I/O module uses sigma-delta A/D conversion to sample and digitize four input channels simultaneously at rates up to 1.0 million samples per second for each channel. The resulting 16-bit sampled data is available to the PCI bus through a 256K-Sample FIFO buffer. Sampling can be controlled in groups of 1 through 4 channels, and the sample clock can be generated from an internal rate generator, or through software, or by external hardware. Both burst and continuous sampling modes are supported. Input ranges are software-selectable as  $\pm 10V$ ,  $\pm 5V$ , or  $\pm 2.5V$ .

Four analog output channels provide software-selected output ranges of  $\pm 2.5V$ ,  $\pm 5V$  or  $\pm 10V$ , independent of the selected analog input range. The outputs are accessed either directly through dedicated control registers, or through a 256K-Sample FIFO buffer for waveform generation. Arbitrary waveform and periodic function generation is supported, as well as realtime function concatenation.

A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports. On-demand autocalibration determines and applies offset and gain correction values for all input and output channels. A selftest input switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host.

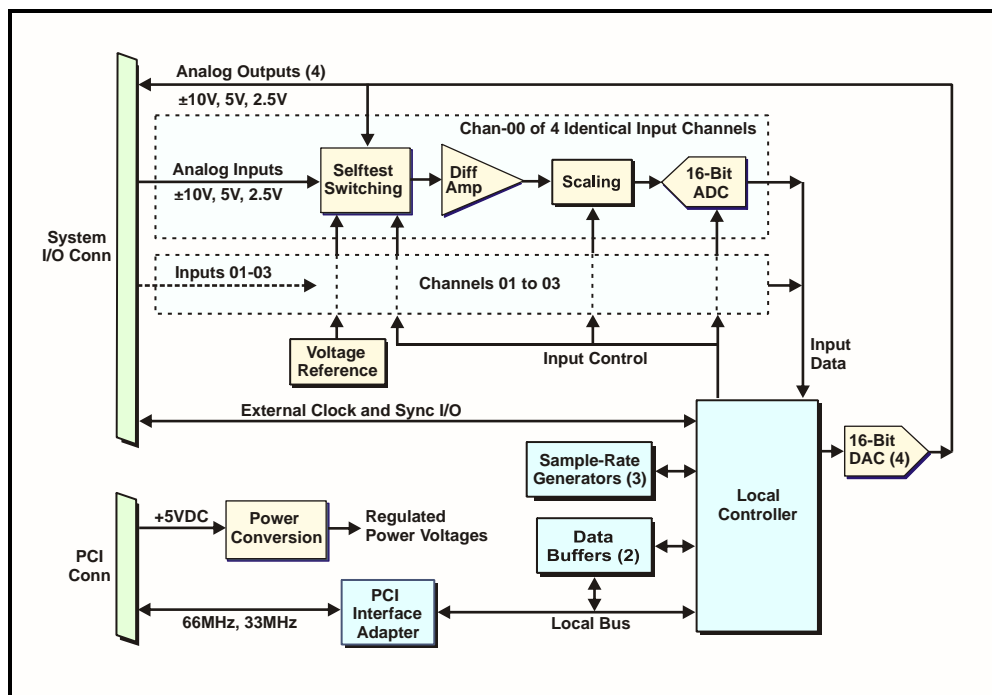


Figure 1. PMC-16HSDI4AO4; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. All operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional air cooling.

## PERFORMANCE SPECIFICATIONS

At +25 °C, with specified operating voltages

### Analog Input Characteristics:

Configuration:	Four differential analog input channels; Dedicated 16-Bit sigma-delta ADC per channel. Optional 2-Channel version available.
Voltage Ranges:	Software-selected as $\pm 10V$ , $\pm 5V$ or $\pm 2.5V$ full scale; Independent of output range.
Input Impedance:	2 Megohms Line-Line in parallel with 40pF.
Bias Current:	100 nanoamps typical all ranges
Crosstalk Rejection:	84dB, DC-10kHz. 70dB at 100kHz.
Common Mode Rejection:	78dB DC-10kHz; 73dB at 100kHz. Typical with CMV = $\pm 10V$ , $V_{in}$ = Zero.
Overvoltage Protection:	$\pm 25V$ with power applied, $\pm 15$ Volts with power removed.

### Analog Input Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Sample Rate:	30KSPS to 1.0MSPS, all channels simultaneously		
Conversion Category:	Sigma-delta.		
Oversampling Factor (OSF):	x32 to 600KSPS; x16 from 600KSPS to 1MSPS		
Sampling Mode::	Simultaneous; all active input channels		
DC Accuracy: (Maximum composite error after autocalibration)	<u>Range</u>	<u>Midscale Accuracy</u>	<u>Fullscale Accuracy</u>
	$\pm 10V$	$\pm 2mV$	$\pm 5mV$
	$\pm 5V$	$\pm 1mV$	$\pm 3mV$
	$\pm 2.5V$	$\pm 0.8mV$	$\pm 2mV$
Small Signal Bandwidth:	Zero to 48-percent of the selected sample rate, -3dB, typical all ranges		
Harmonic Distortion (THD):	93dB to 250kHz with OSF=x32; 91dB to 400kHz with OSF=x16. Typical		
Dynamic Range:	88dB with OSF= x32; 80dB with OSF= x16; Typical on $\pm 10V$ range. (Equivalent to SNR, with fullscale reference)		

### Analog Input Operating Modes and Controls

Input Data Buffer:	256K-sample FIFO
Sample Clock Sources:	Internal rate generator; External Hardware Clock I/O, Software clock.
Sampling Modes:	Continuous sampling or triggered burst.
Sample Rate Generator:	Adjustable PLL oscillator with internal division to the required ADC sample clock.
Trigger Rate Generator:	Programmable from 3-250,000 burst triggers per second, using a 24-Bit divider from the master clock frequency.
External Clock I/O:	TTL, bidirectional. Supports sample rates from 30KSPS to 1.0MSPS.
External Trigger I/O:	TTL, bidirectional. Shared with analog outputs. Supports triggered burst rates from zero to 250KSPS.
Principal Status Register:	Consolidates critical status flags at a single Longword location.
Input Data Format:	16 Bits. Selectable as offset binary or two's complement. First-channel and end-of-burst tagged.

## **Analog Output Characteristics:**

Configuration:	Four single-ended output channels. (Ordering option)
Voltage Ranges:	$\pm 10$ , $\pm 5$ or $\pm 2.5$ Volts; Independent of analog input ranges
Output Resistance:	1.0 Ohm maximum at I/O connector
Output protection:	Withstands sustained short-circuiting to ground
Load Current:	Zero to $\pm 3$ ma per channel
Load Capacitance:	Stable with any load capacitance
Noise:	2.0mV-RMS, 10Hz-100KHz typical
Glitch Impulse:	7 nV-s, typical on $\pm 5$ V range

## **Analog Output Transfer Characteristics:**

Resolution:	16 Bits (0.0015 percent of FSR)												
Output Access:	Direct register access or 256K-Sample FIFO buffer.												
DC Accuracy: (Max error, no-load)	<table border="1"><thead><tr><th>Range</th><th>Midscale Accuracy</th><th><math>\pm</math>Fullscale Accuracy</th></tr></thead><tbody><tr><td><math>\pm 10</math>V</td><td><math>\pm 4</math>mV</td><td><math>\pm 8</math>mV</td></tr><tr><td><math>\pm 5</math>V</td><td><math>\pm 2</math>mV</td><td><math>\pm 6</math>mV</td></tr><tr><td><math>\pm 2.5</math>V</td><td><math>\pm 1.5</math>mV</td><td><math>\pm 4</math>mV</td></tr></tbody></table>	Range	Midscale Accuracy	$\pm$ Fullscale Accuracy	$\pm 10$ V	$\pm 4$ mV	$\pm 8$ mV	$\pm 5$ V	$\pm 2$ mV	$\pm 6$ mV	$\pm 2.5$ V	$\pm 1.5$ mV	$\pm 4$ mV
Range	Midscale Accuracy	$\pm$ Fullscale Accuracy											
$\pm 10$ V	$\pm 4$ mV	$\pm 8$ mV											
$\pm 5$ V	$\pm 2$ mV	$\pm 6$ mV											
$\pm 2.5$ V	$\pm 1.5$ mV	$\pm 4$ mV											
Settling Time:	2.0us to 0.1 percent, typical with halfscale step, no-load. (2.5us for the extended temperature option)												
Crosstalk Rejection:	70 dB minimum, DC-100 kHz												
Integral Nonlinearity:	$\pm 0.007$ percent of FSR, maximum												
Differential Nonlinearity:	$\pm 0.002$ percent of FSR, maximum												
Output Data Format:	16 Bits. Same format as selected for analog inputs.												

## **Analog Output Operating Modes and Controls**

Output Data Buffer:	256K-sample FIFO
Sample Clock Sources:	Internal rate generator; External Clock I/O, Software clock. Or, the output rate clock can be synchronized to the analog input conversion rate.
Burst Triggering Sources:	TTL external Trigger I/O; Internal rate generator (shared with analog inputs), Software trigger.
Clocking Modes:	Continuous or periodic clocking, and triggered burst.
Internal Rate Generator:	Programmable from 3-1,000,000 output clocks per second. Divides Master Clock frequency to clocking rate using a 24-bit divider.
External Clock I/O:	TTL, bidirectional. Zero to 1,000,000 sample clocks per second.
Output Data Format:	16-Bits. Selectable as offset binary or two's complement.

## **Master Clock Frequency Deviation Control:**

Optional feature permits software-controlled  $\pm 50$ PPM deviation of the master clock frequency.

## **Digital I/O Port:**

Dual Independent 8-Bit bidirectional I/O ports. Standard TTL levels. Direct register Access.  $\pm 8$  mA loading when configured as outputs. 0.15 mA source when configured as inputs.

## **PCI Compatibility:**

Conforms to PCI Specification 2.3, D32 read/write, 33/66MHz, universal (5V/3.3V) signaling, Supports block-mode and demand-mode DMA data transfers in two channels as bus master.

## **Power Requirements**

+5VDC  $\pm 0.25$  VDC at 1.5 Amp maximum, 1.1 Amp typical.

Maximum Power Dissipation: Side-1: 6.5 Watts. Side 2: 1.0 Watt.

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## **PHYSICAL PARAMETERS**

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### ***Mechanical Characteristics (PMC Form Factor)***

Height: 13.5 mm (0.53 in)  
Depth: 149.0 mm (5.87 in)  
Width: 74.0 mm (2.91 in)  
Shield: Side-1 is protected by an EMI shield.

### ***Environmental Specifications***

Ambient Temperature Range:  
Standard Temperature: Operating: 0 to +65 Degrees Celsius inlet air  
Storage: -40 to +85 Degrees Celsius  
Extended Temperature: Operating: -40 to +80 Degrees Celsius inlet air  
(Specify with "I" P/N suffix) Storage: -40 to +85 Degrees Celsius  
Relative Humidity: Operating: 0 to 80%, non-condensing  
Storage: 0 to 95%, non-condensing  
Altitude: Operation to 10,000 ft.  
Cooling: Conventional air cooling; 150 LFPM

## ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number **PMC66-16HSDI4AO4-4-4 -44.00M-I** describes a PMC module with eight input channels, four output channels, a 44.000MHz master clock frequency, and Extended Temperature ('industrial') operating range.

in native form factors.

Basic Model Number	Form Factor
PMC66-16HSDI4AO4	PMC (Native)
PCI66-16HSDI4AO4 <sup>1</sup>	PCI, short length
Cpci66-16HSDI4AO4 <sup>1</sup>	cPCI, 3U
PCle66-16HSDI4AO4 <sup>1</sup>	cPCI, 3U
PC104P66-16HSDI4AO4	PC104-Plus
PCle10466-16HSDI4AO4 <sup>1,2</sup>	PCle, one-lane on PC/104 form factor

<sup>1</sup> Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

<sup>2</sup> PCle104 supports only the PCle bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	4 Input Channels	A = 4
	2 Input Channels	A = 2
Number of Output Channels	4 Output Channels	B = 4
	No Analog Outputs	B = 0
Master Clock Frequency *	40.320MHz	C = 40.32M
	44.000MHz	C = 44.00M
	40.000MHz Voltage-Controlled ±50PPM	C = 40.000VC
Custom Feature	---	D **

\* 40.320MHz if both 'C' and 'D' fields are blank.  
Custom frequencies available from 40-44MHz. Contact Sales for details.

\*\* Numeric code, determined by specific feature. Blank or zero (0) if no custom feature applies.

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# SYSTEM INTERFACE CONNECTOR

Table 1. System I/O Connector

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	OUTPUT RTN	1	DIGITAL RTN
2	ANA OUT 00	2	DIO 00
3	OUTPUT RTN	3	DIGITAL RTN
4	ANA OUT 01	4	DIO 01
5	OUTPUT RTN	5	DIGITAL RTN
6	ANA OUT 02	6	DIO 02
7	OUTPUT RTN	7	DIGITAL RTN
8	ANA OUT 03	8	DIO 03
9	INPUT RTN	9	DIGITAL RTN
10	INPUT RTN	10	DIO 04
11	INP00 LO	11	DIGITAL RTN
12	INP00 HI	12	DIO 05
13	INPUT RTN	13	DIGITAL RTN
14	INPUT RTN	14	DIO 06
15	INP01 LO	15	DIGITAL RTN
16	INP01 HI	16	DIO 07
17	INPUT RTN	17	DIGITAL RTN
18	INPUT RTN	18	DIO 08
19	INP02 LO	19	DIGITAL RTN
20	INP02 HI	20	DIO 09
21	INPUT RTN	21	DIGITAL RTN
22	INPUT RTN	22	DIO 10
23	INP03 LO	23	DIGITAL RTN
24	INP03 HI	24	DIO 11
25	INPUT RTN	25	DIGITAL RTN
26	INPUT RTN	26	DIO 12
27	INPUT RTN	27	DIGITAL RTN
28	INPUT RTN	28	DIO 13
29	INPUT RTN	29	DIGITAL RTN
30	INPUT RTN	30	DIO 14
31	INPUT RTN	31	DIGITAL RTN
32	INPUT RTN	32	DIO 15
33	INPUT RTN	33	VTEST RTN
34	INPUT RTN	34	VTEST
35	INPUT RTN	35	DIGITAL RTN
36	INPUT RTN	36	OUTPUT CLK I/O
37	INPUT RTN	37	DIGITAL RTN
38	INPUT RTN	38	TRIGGER I/O
39	INPUT RTN	39	DIGITAL RTN
40	INPUT RTN	40	INPUT CLK I/O

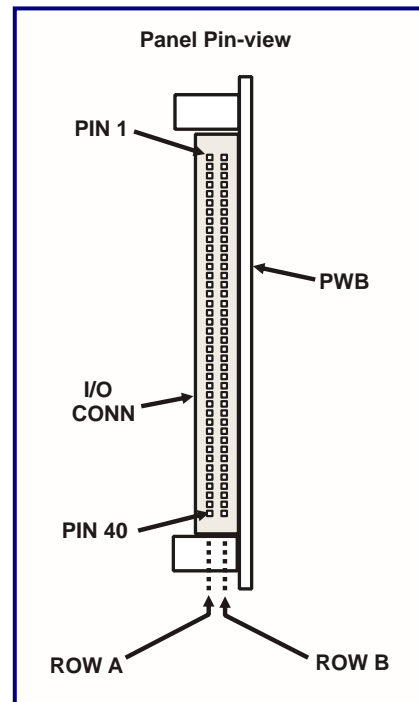


Figure 2. System I/O Connector

**System Mating Connector:**

Standard 80-pin 0.050" dual-ribbon socket:  
Robinson Nugent **P50E-080S-TG**, or equivalent.

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