North Atlantic Industries Apex Signal Division	**Model VME-64CS3**
	Eight (8) S/D and Six (6) D/S Channels

Eight (8) S/D and Six (6) D/S

Two-Speed or Single-Speed or Combination (Programmable)
On-Board Reference
TO COMMERCIAL OR MILITARY SPECIFICATIONS

- 16-bit resolution (24 bits for combined outputs)
- 1 arc-minute accuracy for S/D channels;
- 30 arc-seconds accuracy for D/S channels
- Continuous background BIT testing with Reference and Signal loss detection
- **S/D channels are self-calibrating**. Does not require removal for calibration.
- 47 Hz to 10 kHz operation for S/D channels
- 360 Hz to 10 kHz operation for D/S channels
- S/D tracking rate to 150 RPS
- Transformer isolated
- 1.2 VA D/S drive capability
- 8 and 4-channel S/D versions available
- 6, 4, and 2-channel D/S versions available
- Programmable 2-speed ratios (2 to 255) and D/S angle rotation
- Power-On Self-Test (POST)
- Accurate Digital Velocity outputs
- D/S outputs can be turned ON/OFF
- Optional Encoder (A & B) plus Index outputs; Programmable
- Optional Equivalent A, B, & C Hall Effect commutation outputs
- Optional on-board programmable reference supply
- Optional programmable Synchro/Resolver mode
- LATCH feature
- Either A32, A24 or A16 address
- Geographical addressing
- Synthetic reference for S/D compensates for ±60° phase shift

DESCRIPTION:

This high density DSP-based card contains eight separate transformer isolated Synchro/Resolver-to-Digital tracking converters, six separate transformer isolated Digital-to-Synchro/Resolver converters (1.2 VA), optional 5 VA reference, and extensive diagnostics. All channels also produce differential incremental encoder (A&B) outputs (with programmable resolution) and a zero degree marker pulse or Commutation outputs for 4, 6, or 8 pole brushless DC motors that eliminate the need for Hall Effect sensors on the motor, thus eliminating processor time and reducing bus traffic. The measurement channels incorporate high linearity digital velocity outputs, angle change alert and can be field configured for either single-speed or multi-speed to any ratio between 2 and 255. Ambiguity circuits maintain monotonic outputs by compensating for misalignment between the Coarse and Fine Synchros and the processor will set a flag when it senses that the maximum allowable misalignment of 90°/gear ratio is exceeded.

The S/D channels, even when large accelerations are encountered, never lose tracking, because they incorporate the unique capability to automatically shift to higher bandwidths. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 RPS, at 16-bit resolution. The LATCH feature permits the user to read all channels at the same time. Reading will unlatch the channel. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, assure that current valid data is always available for any channel without effecting the tracking performance of the converters. The Stimulus channels include ON/OFF output capability, common or separate reference inputs, two-speed programmability, and rotation with start and stop angles. The Stimulus channels offer short circuit protection and the ability to ground one of the

outputs without effecting performance. External amplifiers can be added to drive up to 30 VA with a frequency range of 50 to 400 Hz. Each channel can be specified for a different voltage, frequency or resolution.

If geographical addressing is part of the overall system, this card will respond, otherwise the board DIP switches will be activated to set base address. To simplify logistics, Part Number, S/N, Date Code, and Revision are located in permanent memory locations.

Major diagnostics are incorporated to offer substantial improvements to system reliability, because user is alerted to channel malfunctions. This approach also reduces bus traffic because the Status Registers do not require constant polling. Power-On Self-Test (POST) diagnostic can immediately initiate D3 Test. See Programming Instructions for further details. Three different tests (one on-line and two off-line) can be selected:

The D2 Test initiates automatic background BIT testing. Each channel is checked every 5° to a test accuracy of 0.05° and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The D3 Test initiates a BIT test that disconnects all input channels from the outside and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is required for the D/S channels. Any failure triggers an Interrupt (if enabled). Requires no external programming, and can be enabled or disabled via the bus.

The D0 Test is used to check the card and the VME interface. All input channels are disconnected from the outside world thus allowing user to write any number of angles to the card and then read the data from the VME interface. D/S outputs are programmed the same as for normal operation. External reference is required only for D/S.

Conduction cooling which utilizes a thermal plane and wedge locks, can be specified (See P/N.) A stiffener improves vibration response. Both sides of the board can be conformal coated (See P/N). All "E" boards are cycled from -40°C to +85°C for 24 hours.

S/D SPECIFICATIONS: (Applies to each channel)

Resolution:	16 bits (24 bits for combined outputs)
Accuracy:	±1 arc-minute for single speed inputs and frequencies above 400 hz ±2 arc-minute for single speed inputs and frequency of 60 hz (±1 arc-minute divided by the speed ratio for two-speed inputs)
Tracking Rate:	18.5 RPS max. for 60 Hz versions; 150 RPS max. for 360Hz or greater versions. Referred to Fine input in a two-speed configuration
Bandwidth:	Normal is 10 Hz for 60 Hz version; 40 Hz for 400 Hz versions, and 100 Hz for greater than 1kHz versions. Can be readily customized
Input format:	Synchro, Resolver or programmable. (See part number)
Gear ratio:	Each channel pair is programmable from 2 to 255
Input voltage:	Resolver: 2-28 VL-L Auto-ranging , or 90 VL-L Synchro: 11.8 VL-L , or 90 VL-L Resolver and Synchro are transformer isolated
Input Impedance:	40 kΩ min. up to 28 VL-L , 100 kΩ min. at 90 VL-L
Reference/Input:	2-28Vrms, Auto-ranging or 115Vrms. Transformer isolated.
Reference Zin	100 kΩ min.
Frequency:	47 Hz to 10 kHz (See part number)
Encoder outputs:	Either 12,13,14,15, or 16-bit resolution, (field programmable) and Index marker. 12-bit resolution is equivalent to 1,024 cycles (4,096 transitions) etc. Differential outputs. The encoder resolution is fixed and does not change with speed. (Optional, see P/N).
Commutation outputs:	Equivalent to the A, B, C outputs from Hall Effect Sensors for 4, 6 or 8 pole motors
Angle change alert:	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt (if enabled) is triggered. Default: "Ch. disabled". MSB=180°; Min. differential is 0.05°. Max. differential that can be programmed is 179.9º.
Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Velocity, Digital:	16-bit resolution; Linearity: 0.1%. Scalable to 0.1°/sec resolution.
Wrap around Self Test:	The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions.

D/S SPECIFICATIONS: (Applies to each channel)

Resolution:	16 bits (.0055°)
Accuracy:	30 arc-seconds (.0083°) at 0.3 VA. ±1 arc-minute (.017°) at 1.2 VA worst case.
Output format:	(See part number), transformer isolated
Output voltage:	(See code table and part number).
Output load:	1.2 VA max./Channel. Short circuit protected. (5000 Ω reactive at 90 VL-L Synchro, 90 Ω reactive at 11.8 VL-L Synchro, 110 Ω reactive at 11.8 VL-L Resolver)
Load power calculation:	$\{(VL\text{-}L)^2 \times .75\}/Zso$
Regulation:	5% max. No load to Full load
Ratio:	Set any ratio between 2 and 255
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 RPS with a resolution of 0.15°/sec. Step size is 16 bits (0.0055)° up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS
Reference input voltage:	(See part number), Transformer isolated. Uses 1 ma max/Channel
Reference frequency:	360 Hz to 10 kHz (See part number)
Phase shift:	5° max. between output and reference.
Settling time:	Less than 100 microseconds

REFERENCE SUPPLY: Optional. (See part number).

Voltage:	2.0-28Vrms programmable, resolution 0.1Vrms, or 115Vrms fixed is standard. Accuracy ±2%
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5VA max. @ 40° min. inductive; 190mA RMS @ 2-26VAC, 45mA RMS @ 115VAC Note: Power is reduced linearly as the Reference Voltage.

Note: Reference connects only to P2-11a/13a. To interconnect with the S/D and/or D/S channels, see P/N

GENERAL SPECIFICATIONS:

VME Data transfer:	Data transfers within 200 ns.
Interrupts:	One Interrupt capability is implemented. One of seven priority lines can be specified.
Power:	+ 5 VDC at 0.4 A ±12 VDC at 0.8 A nominal, 2.4 A max. (for 8 S/D & 6 D/S channels). Power supplies must be able to supply the peak power without current limiting
Temperature, operating:	"C" =0°C to +70°C, "E" =-40°C to +85°C (See part number)
Storage temperature:	-55°C to +105°C.
Size:	6U (9.2") height, 4HP (0.8") width. 233.4 mm x 20.3 mm x 160 mm deep
Weight:	25 oz.

PROGRAMMING INSTRUCTIONS:

This card offers many options. Any option that is not required may be ignored. For two-speed applications we generally refer to Coarse and Fine channels. Therefore, channel 1 becomes 1 Coarse, channel 2 becomes 1 Fine, channel 3 becomes 2 Coarse, etc.

I/O CONFIGURATION:

The VMEbus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

A32 mode: Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 256 byte boundaries.

A24 mode: Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 256 byte boundaries.

A16 mode: Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 256 byte boundaries.

Enable Geographical Addressing by removing jumper from JP2. Disable Geographical Addressing by adding jumper to JP2.

Geographical Addressing: When Geographical Addressing is enabled, the card will respond to address modifier 2Fh for A24 Address mode, where the 5 MSBs of the A24 address are the 5 bits defined by the slot in VME back plane. The Card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using the address modifier 2Fh, the following need to be written to the card:

1) the base address the card should respond to
2) the address modifier (A16, A24, A32)
3) then enable the card.

For example : If the card is in slot # 10 the 5 MSBs are 01010 so the address of the CSR Registers are :
0101 0 111 1111 1111 xxxx xxxx or 57FFxxh (xx is CSR Register offset)
Write to address 57FF63h, the A31 – A24 base address bits , for example 01h
Write to address 57FF67h, the A23 – A16 base address bits, for example 02h
Write to address 57FF6Bh, the A15 – A8 base address bits, for example 04h
Write to address 57FF6Fh the address modifier you wish to respond to shifted up 2 bits,
for example 28h(0A<< 2)

Then Write to address 57FFFBh , 10h to enable the card.

The card will now respond to the base address (010204 in the example) and address modifier (0Ah in example) programmed. The base address and address modifier can be changed at any time.

MEMORY MAP

00	S/D Ch.1 Data	read	50	Synchro/Resolver	read/write	A4	Stop angle Ch.3	read/write
02	S/D Ch.2 Data Hi	read	52	Power-On (POST) enable **S/D**	read/write	A6	Stop angle Ch.4	read/write
04	S/D Ch.3 Data	read	54	Angle Change Alert	read	A8	Stop angle Ch.5	read/write
06	S/D Ch.4 Data Hi	read	56	(A&B) resolution/poles Ch. 1	read/write	AA	Stop angle Ch.6	read/write
08	S/D Ch.5 Data	read	58	(A&B) resolution/poles Ch. 2	read/write	AC	Rotation rate, D/S Ch.1	read/write
0A	S/D Ch.6 Data Hi	read	5A	(A&B) resolution/poles Ch. 3	read/write	AE	Rotation rate, D/S Ch.2	read/write
0C	S/D Ch.7 Data	read	5C	(A&B) resolution/poles Ch. 4	read/write	B0	Rotation rate, D/S Ch.3	read/write
0E	S/D Ch.8 Data Hi	read	5E	(A&B) resolution/poles Ch. 5	read/write	B2	Rotation rate, D/S Ch.4	read/write
10	Velocity, S/D Ch.1	read	60	(A&B) resolution/poles Ch. 6	read/write	B4	Rotation rate, D/S Ch.5	read/write
12	Velocity, S/D Ch.2	read	62	(A&B) resolution/poles Ch. 7	read/write	B6	Rotation rate, D/S Ch.6	read/write
14	Velocity, S/D Ch.3	read	64	(A&B) resolution/poles Ch. 8	read/write	B8	Rotation, Initiate	write
16	Velocity, S/D Ch.4	read	66	Velocity, S/D scale Ch.1	read/write	BA	Rotation, Stop	write
18	Velocity, S/D Ch.5	read	68	Velocity, S/D scale Ch.2	read/write	BC	Rotation Mode	read/write
1A	Velocity, S/D Ch.6	read	6A	Velocity, S/D scale Ch.3	read/write	BE	Reserved	
1C	Velocity, S/D Ch.7	read	6C	Velocity, S/D scale Ch.4	read/write	C0	Status, Signal **D/S**	read
1E	Velocity, S/D Ch.8	read	6E	Velocity, S/D scale Ch.5	read/write	C2	Status, Reference **D/S**	read
20	Ratio S/D Ch.1/2	read/write	70	Velocity, S/D scale Ch.6	read/write	C4	Status, Test **D/S**	read
22	Ratio S/D Ch.3/4	read/write	72	Velocity, S/D scale Ch.7	read/write	C6	Status, External Amplifier	read
24	Ratio S/D Ch.5/6	read/write	74	Velocity, S/D scale Ch.8	read/write	C8	Test (D2) verify, **D/S**	read/write
26	Ratio S/D Ch.7/8	read/write	78	S/D Ch.2 Data Lo	read	CA	Test Enable, **D/S**	read/write
28	Angle Δ Ch.1	read/write	7A	S/D Ch.4 Data Lo	read	CC	Power-On (POST) enable **D/S**	read/write
2A	Angle Δ Ch.2	read/write	7C	S/D Ch.6 Data Lo	read	CE	Interrupt vector, **D/S**	read/write
2C	Angle Δ Ch.3	read/write	7E	S/D Ch.8 Data Lo	read	D0	Active channels, **D/S**	read/write
2E	Angle Δ Ch.4	read/write	80	D/S Ch.1 Data	write	D2	**D/S** Outputs ON/OFF	read/write
30	Angle Δ Ch.5	read/write	82	D/S Ch.2 Data	write	D4	Internal/External **D/S**	read/write
32	Angle Δ Ch.6	read/write	84	D/S Ch.3 Data	write	EC	Freq. (Ref. Supply)	read/write
34	Angle Δ Ch.7	read/write	86	D/S Ch.4 Data	write	EE	Eo (Ref. Supply)	read/write
36	Angle Δ Ch.8	read/write	88	D/S Ch.5 Data	write	F0	Watchdog timer	read/write
38	Angle Δ initiate	read/write	8A	D/S Ch.6 Data	write	F2	Soft reset	write
3A	Active channels, **S/D**	read/write	8C	Wrap-around D/S Ch.1	read	F4	Interrupt level	read/write
3C	Test (D2) verify, **S/D**	read/write	8E	Wrap-around D/S Ch.2	read	F6	Part #	read
3E	Test Enable, **S/D**	read/write	90	Wrap-around D/S Ch.3	read	F8	Serial #	read
40	Status, Signal **S/D**	read	92	Wrap-around D/S Ch.4	read	FA	Date code	read
42	Status, Reference **S/D**	read	94	Wrap-around D/S Ch.5	read	FE	Save	read/write
44	Status, Test **S/D**	read	96	Wrap-around D/S Ch.6	read	FC	Rev level PCB	read
46	Latch	write	98	Ratio, D/S Ch.1/2	read/write	100	Rev. level S/D DSP	read
48	S/D Test angle	read/write	9A	Ratio, D/S Ch.3/4	read/write	102	Rev. level S/D FPGA	read
4A	Two speed lock loss	read	9C	Ratio, D/S Ch.5/6	read/write	104	Rev. level D/S DSP	read
4C	Interrupt Vector 1 **S/D** (failure)	read/write	A0	Stop angle Ch.1	read/write	106	Rev. level D/S FPGA	read
4E	Interrupt Vector 2 **S/D** (Angle Δ)	read/write	A2	Stop angle Ch.2	read/write	108	Rev. level Interface FPGA	read
						114	Board Ready	read

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data (angle)° Hi	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Data (angle)° Lo	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	0	0	0	0	0	0	0	0
Active channels, **D/S**	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
D/S outputs ON/OFF	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Rotation Mode	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Rotation, Initiate	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Rotation, Stop	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Rotation completed	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Rotation, Start/Stop	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Test Enable, **D/S**	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X
Status, Test **D/S**	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Status, Signal **D/S**	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Status, Reference **D/S**	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Status, Ext. amp (BIT)	Amp 1	Amp 2	Amp 3	Amp 4	Amp 5	Amp 6	X	X	X	X	X	X	X	X	X	X
External/Internal	DS1	DS2	DS3	DS4	DS5	DS6	X	X	X	X	X	X	X	X	X	X
Active channels, **S/D**	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	X	X	X	X	X	X	X	X
Latch outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Two-speed lock loss	X	Ch1/2	X	Ch3/4	X	Ch5/6	X	Ch7/8	X	X	X	X	X	X	X	X
Synchro/Resolver	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	X	X	X	X	X	X	X	X
Angle Change Alert	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	X	X	X	X	X	X	X	X
Test Enable, **S/D**	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Status, Test **S/D**	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	X	X	X	X	X	X	X	X
Status, Signal **S/D**	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	X	X	X	X	X	X	X	X
Status, Reference **S/D**	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	X	X	X	X	X	X	X	X
(A&B) resolution/poles	D15	X	X	X	X	X	X	X	X	X	X	X	X	**D2**	**D1**	**D0**
												4 pole	**16 bit**	0	0	0
												6 pole	**15 bit**	0	0	1
												8 pole	**14 bit**	0	1	0
													13 bit	0	1	1
													12 bit	1	0	0

↑ "0"= Encoder
"1"= Commutation

Note 1 –Values are rounded off.

Commutation outputs ↑

Encoder outputs ↑

COMMON FUNCTIONS

At **Power-On** or **System Reset**, all parameters are restored to last saved setup, and if POST is enabled**,** a D3 Test is initiated.

Active Channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the *Active Channel Register* for S/D and for D/S. "1"=active; "0"=not used. Omitting this step will produce false alarms because unused channels will set faults.

Save Setup: Writing 5555h to the *Save Register* can save the current setup. This location will automatically clear to 0000h when the save is completed (within 5 seconds). When save is elected, all parameters are saved, however, any parameter can be changed at will. Saving is optional. If not saved, reenter parameters at each power up. To restore factory shipped parameters, write AAAAh to the *Save Register*, followed by System Reset. Note: After a SAVE or RESTORE, poll the *Save Register* and do not perform any other operation until word is at "0".

S/D FUNCTIONS

Optional Synchro/Resolver Mode: Where applicable, write a "1" or "0" (Synchro = 1; Resolver = 0) to each bit, representing a channel, of *Synchro/Resolver Register*.

S/D Ratio: Enter the desired ratio, as an integer number, in the *S/D Ratio Register* corresponding to the pair of channels to be used for a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

Read: For single speed applications (Ratio=1), read individual channels 1,2,3,4,etc. For two-speed applications, read only channels (2,4,6,8,etc.) for the combined output of 16 bits. For resolution up to 24 bits, read Data LO word, then Data HI word. Data LO word, when read, latches Data HI word.

In two-speed S/D applications, the single speed information (coarse) from the synchro should be connected to the odd channel of the pair. The N-speed information (multi-speed, fine) from the synchro should be connected to the even channel of the pair. The pairs are defined as: CH1 & 2, CH3 & 4, CH5 & 6, or CH7 & 8.

Two-Speed Lock-Loss: The card monitors misalignment between Coarse and Fine angles during two-speed operation. A two-speed lock loss condition exists if the maximum allowable misalignment between the Coarse and Fine angles of 90°/ratio is exceeded. The corresponding bit for that channel pair in the *Two-Speed Lock-Loss Register* will be set to "0".

Latch: Writing the integer 2 to the *Latch Register* will cause the angle data of all the channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

Velocity Output: Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then
Velocity in RPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 RPS

Velocity Scale Factor: The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS),** where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale Register* for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and -32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh;
This results in a velocity resolution of: (152.5878 RPS/32,767) x 360°/RPS = 1.676°/sec (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);
This is a velocity resolution of: (50.8626 RPS/32,767) x 360°/RPS = 0.5588°/sec

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h; 0.10477 °/sec resolution (lowest setting)

Angle Change Alert: Write a 16-bit word to the appropriate *Angle Change Register*, to represent the minimum differential required. MSB=180°; Min. differential is 0.05°, setting to zero disables the Angle Change Alert for a given channel. Initiate monitoring by writing "1" to *Angle Change Initiate Register*.

When that differential is exceeded, on any monitored channel, the bit corresponding to that channel is set in the *Angle Change Alert Register.* ("0" = no change, "1" = change). See Register Bit Map.

Optional (A&B) Encoder Resolution: To set Encoder Mode, write a "0" to the D15 bit and the appropriate code for the desired resolution to the D2, D1 & D0 bits of the corresponding channel (*A&B) Resolution/Poles Register*. Changing the resolution for any channel can be done on the fly. The default is a 12bit resolution encoder output. See Register Bit map table. **Note**: Encoder/Commutation outputs are optional; see part ordering information.

Optional Commutation Outputs (A,B,C): To set Commutation Mode, write a "1" to the D15 bit and the appropriate code for the required motor poles to the D2, D1 & D0 bits of the corresponding channel *(A&B) Resolution/Poles Register*. See Register Bit map table.
Note: Encoder/Commutation outputs are optional; see part ordering information.

S/D Power-On Self-Test (POST): The unit will initiate the D3 Test upon power-on, if POST is enabled and saved. Enable by writing "1" to S/D *POST Register*. Disable by writing "0" to *POST Register* and then save setup.

S/D D2 Test Enable: Writing "1" to the D2 bit of the *S/D Test Enable Register* initiates automatic background BIT testing that checks each channel every 5° to a test accuracy of 0.05°. The result of an accuracy error is available in the *S/D Test Status Register* and if enabled, an interrupt will be generated (See *Interrupt Register*). A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled. The card will write 55h to the *S/D Test (D2) Verify Register*, every 30 seconds, when the D2 Test is enabled. User can periodically clear the *Test (D2) Verify Register* by writing 00h, waiting 30 seconds, then reading the register again to verify that background BIT testing is activated.

In addition, each S/D Signal and Reference input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *S/D Signal* and *Reference Status Registers*.

S/D D3 Test Enable: Writing "1" to the D3 bit of the *S/D Test Enable Register* initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is not required. The test cycle is completed within 45 seconds and results can be read from the *S/D Test Status Registers* when D3 bit changes from "1" to "0" and if enabled, an interrupt will be generated if a BIT failure is detected (See *Interrupt Register*). The testing can be terminated at any time by writing "0" to D3 bit of the *S/D Test Enable Register*.

Signal and Reference monitoring is disabled during D3 test.

S/D D0 Test Enable: Used to check card and the VME interface. Writing "1" to the D0 bit of the *S/D Test Enable Register* disconnects all channels from the outside world and connects them to internal test signals, enabling the user to generate any test angle by writing an integer value, to the *S/D Test Angle Register*. Data is then read through the interface (after writing, allow 400 ms before reading). External reference is not required. (e.g. 330° = angle/(360/2^{16})).

Signal and Reference monitoring is disabled during D0 test.

S/D Status, Test : Check the channel's corresponding bit of the *S/D Test Status Register* for status of BIT testing for each active channel. A "1" means accuracy passes; A "0" indicates a failure on an active channel. Channels that are inactive are also set to "0". (Test cycle takes 45 seconds for accuracy error). Any S/D Test status failure, transient or intermittent will latch the *S/D Test Status Register*. Reading will unlatch register.

S/D Status, Ref : Check the channel's corresponding bit of the *S/D Reference Status Register* for status of the reference input for each active channel. A "1" means Reference ON, a "0" means Reference Loss on active channels. Channels that are inactive are also set to "0". (Reference loss is detected within 2 seconds). Reference monitoring is disabled during D3 or D0 Test. Any S/D Reference status failure, transient or intermittent will latch the *S/D Reference Status Register*. Reading will unlatch register.

S/D Status Signal: Check the channel's corresponding bit of the *S/D Signal Status Register* for status of the input signals for each active channel. A "1" means Signal is valid (level must be a minimum of 2V), a "0" means Signal loss on active channels. (Signal loss is detected after 2 seconds). Channels that are inactive are also set to "0". Signal monitoring is disabled during D3 and D0 test. Any S/D Signal status failure, transient or intermittent will latch the *S/D Signal Status Register*. Reading will unlatch register.

Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. After reading, registers will be updated with the background data within 250ms. Allow 250 ms to scan all channels.

Interrupt Vector 1: Write 8-bit word (0-255) to the *S/D Interrupt Vector 1 Register*. Used for S/D failure reports.

Interrupt Vector 2: Write 8-bit word (0-255) to the *S/D Interrupt Vector 2 Register*. Used for S/D angle change alert reports.

D/S FUNCTIONS

Write Angle – Single Speed:

For single-speed applications (Ratio=1), write a 16-bit integer (or 16-bit 2's compliment integer) to the corresponding channel *D/S Data Register.* (ex. 330° = EAABh).
WORD = (Angle ÷ (360/2^{16})).
Note: writing to an Input Angle Register will stop any rotation initiated on that channel

D/S Ratio: Enter the desired ratio, as an integer number, in the *D/S Ratio Register* corresponding to the pair of channels to be used as a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

Write Angle – Two-Speed:

In two-speed applications, the ratio will affect the fine speed output resolution. (Higher ratios result in lower resolutions at the output.) This occurs from multiplying the coarse angle by the ratio to achieve the fine angle output. This multiply reduces the overall resolution by increasing the weight of the LSB's. To compensate for this, the card allows for 24-bit resolution for the higher ratios. This feature is transparent and automatic to the user and will regain the resolution needed in higher ratio systems.

When 16 bit resolution is sufficient, the angle can be represented by first writing the integer 0 to the even channel of the pair *D/S Data Register,* then a 16-bit integer (or 16-bit 2's compliment integer) to the odd channel

of the pair (coarse speed) *D/S Data Register*. The card will set the angle of second channel output (fine speed), to the coarse angle multiplied by the ratio. Note: Integer 0 only needs to be written to the even channel once to initialize the even channel register. Subsequently, only writes to the odd channel are necessary.

Odd Channel	Even Channel
16 Bits	0

16 bit integer = Angle / ($360/2^{16}$); Fine Speed ≡ Angle * Ratio / ($360/2^{16}$)

Ex1. For a ratio of 255, the fine speed output would have a resolution of 1.4008°.
Thus, for every 0.00549° of shaft angle, the fine output will change in 1.4008° increments.

When 24 bit resolution is desired, the angle can be represented as a 24-bit integer (or 24-bit 2's compliment integer) by first writing the lower 8-bits to the upper byte of the even channel of the pair of the *D/S Data Register*, then the upper 16-bits to the odd channel of the pair (coarse speed) of the *D/S Data Register*. The card will set the angle of second channel output (fine speed), to the coarse angle multiplied by the ratio. The channel pairs are defined as Ch1&2, Ch3&4, Ch5&6 and Ch7&8.

Odd Channel	Even Channel	
16 Bits	8 Bits	X

24 bit integer = Angle / ($360/2^{24}$); Fine Speed ≡ Angle * Ratio / ($360/2^{24}$)

Ex1. For a ratio of 255, the fine speed output would have a resolution of 0.00547°.
Thus, for every 0.000021458° of shaft angle, the fine output will change in 0.00547° increments.

Note: Writing to an input angle register will stop any rotation initiated on that channel.

Outputs ON/OFF: Set the bit corresponding to each channel to be turned on, to "1" in the *Output On/Off Register*. To turn OFF a channel, set corresponding bit to "0". Default: Set to OFF

Read Wrap-Around Angles: Wrap-around angles are read from the *D/S Wrap-around Registers*. Each enabled D/S channel is measured prior to the transformer output and can be read from the corresponding *D/S Wrap-around Register*. The generated result is a 16-bit binary word (or 16-bit 2's compliment word).
The data is available at any time.

Rotation Rate: Write to the corresponding *Rotation Rate Register* a 2's complement number representing the desired rotation rate, LSB = 0.15°/sec.
Ex: 12 RPS =. (12 x 360°/0.15° = 28800 = 7080h), -12 RPS = (-12 x 360°/0.15° = -28800 = 8F80h)
Step size is 16 bits (0.0055°) for up to 1.5 RPS, then linearly decreases to 12 bits (0.088°) at 13.6 RPS.
Rotation Mode, Continuous or Start/Stop: For continuous rotation, set the corresponding channel bit to "0" in the *Rotation Mode Register*. For rotation to cease at a designated stop angle, set the bit to "1".

Stop Angles: Write the desired stop angle to appropriate channel *Stop Angle Register*. After a channel reaches the stop angle, it will stop rotating and remain at that angle until a new input angle is set. If rotation is initiated again, the angle will start rotating from the present angle.

Initiate Rotation: First set the *Rotation Rate* and *Rotation Mode Register* for each channel that is to rotate. Then, to start rotation for those channels, set the corresponding channel bit to a "1" in the *Rotation Initiate Register*.

Stop Rotation: Set the corresponding bit, for each channel to be stopped, to a "1" in the *Rotation Stop Register*. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated.

D/S D2 Test Enable: Writing "1" to the D2 bit of the *D/S Test Enable Register* initiates automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle, before the output transformer, to the commanded angle. The status bits will be set to indicate an accuracy (0.05º) problem and the results can be read from *D/S Status Registers* within 2 seconds and if enabled, an interrupt will be generated (See *Interrupt Register*. A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. Outputs must be ON and Reference supplied for test to function. Card will write 55h (every 2 seconds) to the *D/S Test (D2) Verify Register* when D2 is enabled. User can periodically clear to 00h and then read the *D/S Test (D2) Verify Register* again, after 2 seconds, to verify that BIT Testing is activated. This test continuously sequences between the six channels on the card with each output being measured for approx. 180mSec. If the measured angle has an error greater the 0.05º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error.

In addition, each D/S Reference input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *D/S Signal* and *D/S Reference Status Registers*.

D/S D3 Test Enable: Writing "1" to the D3 bit of the *D/S Test Enable Register* initiates a BIT Test that generates and tests 72 different angles to an accuracy of 0.05°. External reference is required and outputs must be ON. The D/S Status bits will be set to indicate an accuracy problem. Results are available in the *D/S Test Status Registers* and if enabled, an interrupt will be generated (See *Interrupt Register*). Test cycle takes about 30 seconds and the D3 bit changes from "1" to "0" when test is complete. The testing requires no external programming, and can be terminated at any time by writing a "0" to the D3 bit of the *D/S Test Enable Register*. **CAUTION: Outputs must be ON and Reference supplied during this test and is therefore active.** Check connected loads for possible interaction.

D/S Power-On Self-Test (POST): The unit will initiate the D3 Test on Power-On, if POST is enabled and saved. Enable by writing "1" or Disable by writing "0" to D/S *POST Register* and then save setup.

D/S Status, Test: Check the corresponding bit of the *D/S Test Status Register* for status of BIT Testing for each active channel. A "1" means Accuracy OK; "0" failed. Channels that are inactive are also set to "0". (test cycle takes 2 seconds for accuracy error). Any D/S test status failure, transient or intermittent will latch the *D/S Test Status Register*. Reading will unlatch register.

D/S Status, Ref: Check the corresponding bit of the *D/S Reference Status Register* for status of the reference input for each active channel. A "1" means Reference ON, "0" means Reference Loss on active channels. Channels that are inactive are also set to "0". (Reference loss is detected after 2 seconds). Reference monitoring is always enabled. Any D/S reference status failure, transient or intermittent will latch the *D/S Reference Status Register*. Reading will unlatch register.

D/S Status, Sig: Check the corresponding bit of the *D/S Signal Status Register* for status of the input signals for each active channel. A "1" means Signal is valid, "0" means Signal loss. Channels that are inactive are also set to "0". (Signal loss is detected after 2 seconds). Signal monitoring is always enabled. Any D/S Signal status failure, transient or intermittent will latch the *D/S Signal Status Register*. Reading will unlatch register.

D/S Status, Ext. Amp: Check the corresponding bit of the *Ext Amp Status Register*, for status of BIT testing for each active channel that has the External Amp enabled. A "1" =Accuracy OK; "0" =failed. Any D/S Ext Amp status failure, transient or intermittent will latch the *D/S Ext Amp Status Register*. Reading will unlatch register.

External/Internal: When wrap-around BIT test capability is required for external Synchro amplifiers, set the bit, corresponding to each channel that has an external amplifier to be monitored, to "1" in the *External/Internal Register***.** Default is Internal.

Interrupt Vector D/S: Write 16-bit word (0-255) to *D/S Interrupt Vector Register*.

ADDITIONAL COMMON FUNCTIONS

Enter Interrupt Levels: Write a 16-bit binary number to the *Interrupt Level Register*; 0= no interrupt; 1-7 indicates priority levels. Any error will latch the *Status Registers* and trigger an Interrupt. When Interrupt is acknowledged, additional errors will set another Interrupt. Reading will unlatch registers. Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected, latched into registers and subsequent scans find that the reference was reconnected, the status change will be held in background until the registers are read. After reading, registers will be updated with the background data within 250ms.

Soft Reset: (Level sensitive): Writing a "1" to the *Soft Reset Register* initiates and holds software in reset state. Then, writing "0" initiates reboot (takes 400 ms). Following the soft reset, a power on automatic calibration test is run and completes in approximately 30 seconds. This function is equivalent to Power on Reset.

Watchdog Timer: This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µsec. The inverted code stays in the register until replaced by a new code. The user should look for the inverted code, after 100 µsec, to confirm that the processor is operating.

Optional Reference Supply: For frequency, write a 16-bit integer to the *Frequency Ref Supply Register*. (Ex: 400 Hz = 0190h) with LSB= 1Hz. For voltage, write a 16-bit integer to the *Voltage Ref Supply Register*. (Ex: 26Vrms =0104h) with LSB=0.1Vrms. It is recommended that the user program the required frequency before setting the output voltage.

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number: Read as a 16-bit binary word from the *Serial Number Register*. Serial number of purchased board.

Date Code: Read as decimal number from the *Date Code Register*. The four digits represent YYWW (Year, Year, Week, Week).

Rev Levels: There are a total of 6 *Revision Level Registers*. Each register is defined as 16 bits. The integer value of that particular register corresponds to the actual revision.

Board Ready: Poll register. Board is ready to be accessed **only after** you read "AA55". (within 1 second after board power-on)

CONNECTORS:

J1: DC37P; Mate: DC37S

Pin	D/S 1	Pin	D/S 2	Pin	D/S 3	Pin	D/S 4	Pin	**WA 1**	Pin	**WA 3**
37	S1	34	S1	31	S1	28	S1	25	Cosine	22	Cosine
19	S2	16	S2	13	S2	10	S2	7	Sine	4	Sine
36	S3	33	S3	30	S3	27	S3	6	Comm	3	Comm
18	S4	15	S4	12	S4	9	S4	Pin	**WA 2**	Pin	**WA 4**
35	∗RHi	32	∗RHi	29	∗RHi	26	∗RHi	5	Cosine	2	Cosine
17	∗RLo	14	∗RLo	11	∗RLo	8	∗RLo	24	Sine	21	Sine
						1	Chassis	23	Comm	20	Comm

J2: DC37P; Mate: DC37S

Pin	S/D 1	Pin	S/D 2	Pin	S/D 3	Pin	S/D 4	Pin	S/D 5	Pin	S/D 6
37	S1	34	S1	31	S1	28	S1	25	S1	22	S1
19	S2	16	S2	13	S2	10	S2	7	S2	4	S2
36	S3	33	S3	30	S3	27	S3	24	S3	21	S3
18	S4	15	S4	12	S4	9	S4	6	S4	3	S4
35	∗RHi	32	RHi	29	∗RHi	26	∗RHi	23	∗RHi	20	∗RHi
17	∗RLo	14	RLo	11	∗RLo	8	∗RLo	5	∗RLo	2	∗RLo
										1	Chassis

WA= wrap around from external Amplifier

J3: DB25P; Mate: DB25S

Pin	S/D 7	Pin	S/D 7	Pin	S/D 8	Pin	S/D 8	Pin	D/S 5	Pin	D/S 5	Pin	D/S 6	Pin	D/S 6	Pin	Designation
25	S1	12	S4	22	S1	9	S4	19	S1	6	S4	16	S1	3	S4	1	Chassis
13	S2	23	∗RHi	10	S2	20	∗RHi	7	S2	17	∗RHi	4	S2	14	∗RHi		
24	S3	11	∗RLo	21	S3	8	∗RLo	18	S3	5	∗RLo	15	S3	2	∗RLo		

P2 Connector

Pin	Designation	Pin	Designation	Pin	Designation	Pn	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation
18c	S1 SD 1	32c	S3 SD 3	1z	∗RLo SD 5	22d	S1 SD 8	3a	S3 DS 2	7c	∗RLo DS 4	3z	WA Cos 1
20c	S2 SD 1	31c	S4 SD 3	1d	∗RHi SD 5	23d	S2 SD 8	3c	S4 DS 2	7a	∗RHi DS 4	5z	WA sin 1
22c	S3 SD 1	32a	∗RLo SD 3	14d	S1 SD 6	24d	S3 SD 8	1c	∗RLo DS 2	2d	S1 DS 5	7z	Common 1
24c	S4 SD 1	31a	∗RHi SD 3	15d	S2 SD 6	23c	S4 SD 8	1a	∗RHi DS 2	3d	S2 DS 5	9z	WA Cos 2
27c	∗RLo SD 1	18a	S1 SD 4	16d	S3 SD 6	27d	∗RLo SD 8	5a	S1 DS 3	4d	S3 DS 5	11z	WA sin 2
29c	∗RHi SD 1	20a	S2 SD 4	17d	S4 SD 6	28d	∗RHi SD 8	5c	S2 DS 3	5d	S4 DS 5	13z	Common 2
10c	S1 SD 2	22a	S3 SD 4	29d	∗RLo SD 6	10a	S1 DS 1	6a	S3 DS 3	25a	∗RLo DS 5	15z	WA Cos 3
12c	S2 SD 2	24a	S4 SD 4	30d	∗RHi SD 6	12a	S2 DS 1	6c	S4 DS 3	26a	∗RHi DS 5	17z	WA sin 3
14c	S3 SD 2	29a	∗RLo SD 4	18d	S1 SD 7	14a	S3 DS 1	4c	∗RLo DS 3	6d	S1 DS 6	19z	Common 3
16c	S4 SD 2	30a	∗RHi SD 4	19d	S2 SD 7	16a	S4 DS 1	4a	∗RHi DS 3	7d	S2 DS 6	21z	WA Cos 4
30c	∗RLo SD 2	10d	S1 SD 5	20d	S3 SD 7	27a	∗RLo DS 1	8a	S1 DS 4	8d	S3 DS 6	23z	WA sin 4
28c	∗RHi SD 2	11d	S2 SD 5	21d	S4 SD 7	28a	∗RHi DS 1	8c	S2 DS 4	9d	S4 DS 6	25z	Common 4
25c	S1 SD 3	12d	S3 SD 5	27z	∗RLo SD 7	2a	S1 DS 2	9a	S3 DS 4	25d	∗RLo DS 6	11a	Ref. Out Hi
26c	S2 SD 3	13d	S4 SD 5	29z	∗RHi SD 7	2c	S2 DS 2	9c	S4 DS 4	26d	∗RHi DS 6	13a	Ref. Out Lo

S4 pins used only with Resolvers.

∗These pins are connected as per P/N Option specified. When common references are specified, active pins for the S/D Channels would be at 29c/27c (J2-35/17) and for the D/S channels at 28a/27a. (J1-35/17)

NOTE: P2 is always active.

P0 Connector:

1e	Ch.1 A Hi	3b	Ch.3 A Lo	7e	On/Off Hi Ch.2	13d	BIT Lo Ch. 2	19d	WA sin 6	17c	Ch.6 Index Lo
1d	Ch.1 A Lo	3c	Ch.3 B Hi	7d	On/Off Lo Ch.2	14e	BIT Hi Ch. 3	19c	common 6	6b	Ch.7 A Hi
1a	Ch.1 B Hi	4c	Ch.3 B Lo	8e	On/Off Hi Ch.3	14d	BIT Lo Ch. 3	6c	Ch. 5 A Hi	7b	Ch.7 A Lo
1b	Ch.1 B Lo	4b	Ch.3 Index Hi	8d	On/Off Lo Ch.3	15e	BIT Hi Ch. 4	7c	Ch. 5 A Lo	8b	Ch.7 B Hi
1c	Ch.1 Index Hi	4a	Ch.3 Index Lo	9e	On/Off Hi Ch.4	15d	BIT Lo Ch. 4	8c	Ch. 5 B Hi	9b	Ch.7 B Lo
2c	Ch.1 Index Lo	4d	Ch.4 A Hi	9d	On/Off Lo Ch.4	16e	BIT Hi Ch. 5	9c	Ch. 5 B Lo	10b	Ch.7 Index Hi
2b	Ch.2 A Hi	4e	Ch.4 A Lo	10e	On/Off Hi Ch.5	16d	BIT Lo Ch. 5	10c	Ch.5 Index Hi	11b	Ch.7 Index Lo
2a	Ch.2 A Lo	5e	Ch.4 B Hi	10d	On/Off Lo Ch.5	17e	BIT Hi Ch. 6	11c	Ch.5 Index Lo	12b	Ch.8 A Hi
2d	Ch.2 B Hi	5d	Ch.4 B Lo	11e	On/Off Hi Ch.6	17d	BIT Lo Ch. 6	12c	Ch.6 A Hi	13b	Ch.8 A Lo
2e	Ch.2 B Lo	5a	Ch.4 Index Hi	11d	On/Off Lo Ch.6	18e	WA Cos 5	13c	Ch.6 A Lo	14b	Ch.8 B Hi
3e	Ch.2 Index Hi	5b	Ch.4 Index Lo	12e	BIT Hi Ch. 1	18d	WA sin 5	14c	Ch.6 B Hi	15b	Ch.8 B Lo
3d	Ch.2 Index Lo	6e	On/Off Hi	12d	BIT Lo Ch. 1	18c	common 5	15c	Ch.6 B Lo	16b	Ch.8 Index Hi
3a	Ch.3 A Hi	6d	On/Off Lo	13e	BIT Hi Ch. 2	19e	WA Cos 6	16c	Ch.6 Index Hi	17b	Ch.8 Index Lo

NOTE: For commutation (A, B, C) outputs: A Hi becomes A, B Hi becomes B, and Index Hi becomes C.
The board contains two green LED's that are for factory use only. The two-miniature test connectors are used to download programming data. Do not interface to these two connectors unless factory instructed. Used for field modification.

Code Table

Code		Input (V_{L-L})	Ref (Vrms)	Freq (Hz)	Optional On-Board Reference Output[1]	Output (V_{L-L})	Ref (Vrms)	Freq (Hz)	Load	Notes
01		11.8	26	400	2-28Vrms	11.8	26	400	1.2 VA	
02		90	115	400	115Vrms	90	115	400	1.2 VA	
03		90	115	50/400	115Vrms	90	115	400	1.2 VA	

Note 1 - Applicable only when ordering On-Board reference
See code list addendum for descriptions of code 50 and above

PART NUMBER DESIGNATION

64CS3 X X X X X X - XX

TOTAL NUMBER OF S/D CHANNELS
0 = 0 S/D Channels
4 = 4 S/D Channels
8 = 8 S/D Channels

TOTAL NUMBER OF D/S CHANNELS
0 = 0 D/S Channels
2 = 2 D/S Channels
4 = 4 D/S Channels
6 = 6 D/S Channels

ENVIRONMENTAL
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating
contact factory for other temperature requirements

FORMAT
S = Synchro
R = Resolver
M = Mixed (See Code Table)
P = Programmable Synchro/Resolver (measurement)

CODE (See Code Table)

ENCODER/COMMUTATION
- = Without Encoder/Commutation option
E = With Encoder/Commutation option

OPTIONS

With On-Board Reference:
1 = Connected ONLY to P2-11a/13a. Separate S/D and D/S Reference Input.
2 = Connected to Common D/S and to Separate S/D Reference Inputs.
3 = Connected to Common S/D and to Separate D/S Reference Inputs.
4 = Connected to Common S/D, to Common D/S and to P2.

Without On-Board Reference:
5 = Common D/S. Separate S/D Reference Inputs.
6 = Common S/D. Separate D/S Reference Inputs.
7 = Common S/D Connected to Common D/S.
8 = Separate S/D and D/S Reference Inputs.

Custom Design:
9 = Custom Design (See Separate Spec)

MECHANICAL
F = Front Panel I/O and P2 I/O
P = P2 I/O only
W =P With Wedgelocks
A =VME64 with Blank Front Panel and P2 I/O only
B =VME64 Front Panel with Front Panel I/O & P2 I/O
D =VME64 with Blank Front Panel, Low profile extractors and P2 I/O only

Revision Page

Revision	Description of Change	Engineer	Date
4.2	Added pg. 13 (rev page); Corrected definition of 24-bit 2 speed S/D read LO then HI (pg. 5); Corrected memory map offsets for Data LO S/D CH2,4,6,8 (pg. 4)	ARS	14 Oct 05
4.3	Corrected typo. Pg 9, D/S Status, Sig description	FR	14 Jul 06
4.4	New Address	KL	24 April 07