



Sixteen (16) Synchro/Resolver-to-Digital Channels

## **Sixteen (16) Synchro/Resolver-to-Digital**

### **Two-Speed or Single-Speed or Combination (Programmable)**

### **On-Board Programmable Reference Supply**

To Commercial or Military Specifications

- 16-bit resolution (24 bits combined)
- $\pm 1$  arc-minute accuracy for single speed
- Continuous background BIT testing with Reference and Signal loss detection
- **Self-calibrating. Does not require removal for calibration**
- 50 Hz to 10 kHz operation
- Tracking rate to 150 RPS
- 16, 12, 8, and 4-channel versions available
- Programmable 2-speed ratios: 2 to 255
- Accurate Digital Velocity outputs
- Optional programmable encoder (A & B) plus index outputs
- Optional equivalent Hall Effect (A, B, C) commutation outputs
- Optional on-board programmable reference supply
- Watchdog timer and soft reset
- Angle change alert
- Galvanic Isolation
- Synthetic reference compensates for  $\pm 60^\circ$  phase shift
- Optional conduction cooling with wedgelocks
- I/O via front panel, P2 or both
- Latch feature (Hardware & Software)
- No adjustments or trimming required
- Part Number, S/N, Date Code, & Revision in non-volatile memory

### **DESCRIPTION:**

This high density intelligent DSP-based card incorporates up to sixteen (16) single-speed or eight (8) two-speed transformer isolated Synchro/Resolver-to-Digital tracking converters with extensive diagnostics, digital velocity outputs, angle change alert, and optional programmable reference supply. Any combination of two-speed and single-speed channels can be field programmed to any ratio between 2 and 255. Each channel also produces differential (A & B) incremental encoder outputs (with programmable resolution) and a zero degree marker pulse. Alternatively, commutation outputs are available for 4, 6, or 8 pole brushless DC motors that eliminate the need for Hall Effect sensors on the motor. For 2-speed usage, ambiguity circuits maintain monotonic outputs by compensating for misalignment between the Coarse and Fine Synchros. However, the processor will set a flag when it senses that the maximum allowable misalignment of  $90^\circ$ /gear ratio is exceeded.

This card, even when large accelerations are encountered, never loses tracking, because it incorporates the unique capability to automatically shift to higher bandwidths. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 RPS, at 16-bit resolution. Both a software and hardware LATCH feature is provided to permits the user to read all channels at the same time. Reading will unlatch that channel. The angle alert monitors each channel for the programmed angle difference and sets an interrupt as soon as that threshold is reached. Thus, no polling of the angle registers is required until an angle has reached the specified difference. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that valid data is always available. Our synthetic reference compensates for  $\pm 60^\circ$  phase shifts, thus eliminating the need for individual compensation networks. A watchdog timer is provided to monitor the processor. Part number, S/N, Date Code and Revision are located in non-volatile memory.

Conduction cooling which utilizes a thermal plane and wedge locks, can be specified (See P/N). The heat sink also serves as a stiffener that improves vibration response. Both sides of the board can be conformal coated (See P/N). All "E" boards are cycled from -40°C to +85°C for 24 hours.

This board incorporates major diagnostics that offer substantial improvements to system reliability, because the user is alerted to any channel malfunction. Three different tests, one on-line and two off-line, can be selected:

The (D2) Test initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled via the bus.

The (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. Results can be read from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped via the bus.

The (D0) Test is used to check the card and the VME interface. All channels are disconnected from the outside world, allowing the user to write any number of input angles to the card and then to read the data from the interface. External reference is not required.

## **SPECIFICATIONS:**

Resolution:	16 bits (up to 24 bits for two-speed configuration)
Accuracy:	±1 arc-minute for single speed inputs ±1 arc-minute divided by the gear ratio for two-speed inputs
VME Data transfer:	Data transfers within 200 ns.
Tracking Rate:	18.5 RPS for 60 Hz version; 150 RPS for 360 Hz or greater versions. (Referred to the Fine input for two-speed configuration)
Bandwidth:	10 Hz for 60 Hz versions; 40 Hz for 400 Hz versions, & 100 Hz for greater than 1 kHz version. (also can be factory customized)
Input format:	Synchro or Resolver, (see part number)
Gear ratio:	Each channel pair is programmable from 2 to 255
Input voltage:	Resolver: 2-28 V <sub>L-L</sub> Autoranging, or 90 V <sub>L-L</sub> ; Synchro: 11.8 V <sub>L-L</sub> , or 90 V <sub>L-L</sub> Resolver and Synchro are Transformer isolated
Input Impedance:	40 kΩ min. up to 28 V <sub>L-L</sub> , 100 kΩ min. at 90 V <sub>L-L</sub>
Reference:	2-28 Vrms, Autoranging or 115 Vrms. Transformer isolated.
Reference Zin	100 kΩ min.
Frequency:	47 Hz to 10 kHz (see part number)
Encoder outputs:	Either 12,13,14,15, or 16-bit resolution, (field programmable) and Index marker. 12-bit resolution is equivalent to 1,024 cycles (4,096 transitions) etc. Differential outputs. The encoder resolution is fixed and does not change with speed. (Optional, see P/N).
Commutation outputs:	Equivalent to the A, B, C outputs from Hall Effect Sensors for 4, 6 or 8 pole motors
Angle change alert:	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt (if enabled) is triggered. Default: "Ch. Disabled". MSB=180°; Min. differential is 0.05°. Max differential that can be programmed is 179.9°.
Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Velocity, Digital:	16-bit resolution; Linearity: 0.1%. Scalable to 0.1°/sec resolution.
Wrap around Self Test:	The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions.
Interrupts:	One Interrupt capability is implemented. One of seven priority lines can be specified.
Power:	+ 5 VDC: 0.350 A for 16 channels; ±12 VDC: 0.08 A without Reference; .600 A with 5 VA out.
Temperature, operating:	"C" 0°C to +70°C; "E" -40°C to +85°C (see part number)
Storage temperature:	-55°C to +105°C.
Conformal coating:	Both sides of the board can be conformal coated (see part number).
Temperature Cycled:	All "E" boards are cycled from -40°C to +85°C for 24 hours.
Size:	6U (9.2") height, 4HP (0.8") width. 233.4 mm x 20.3 mm x 160 mm deep
Weight:	22 oz.

**REFERENCE SUPPLY:** Optional. (see part number).

Voltage: 2.0-28 Vrms programmable (resolution 0.1 Vrms) or 115 Vrms fixed. Accuracy ±2%.  
 Frequency: 360 Hz to 10 kHz ±1% with 1 Hz resolution.  
 Regulation: 10% max. No load to full load.  
 Output power: 5 VA max. at 40° min. inductive.

**PROGRAMMING INSTRUCTIONS:**

This card offers many options. Any option that is not required may be ignored. For ease of use, all channels are referred to as 1 to 16. For two-speed applications, we generally refer to Coarse and Fine inputs. Therefore, channel 1 becomes 1 Coarse, channel 2 becomes 1 Fine, channel 3 becomes 2 Coarse, etc.

**I/O CONFIGURATION:**

The VMEbus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

**A32 mode:** Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 256 byte boundaries (Standard), or 512 byte boundaries, when offset addresses above 100 are enabled.

**A24 mode:** Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 256 byte boundaries (Standard), or 512 byte boundaries, when offset addresses above 100 are enabled

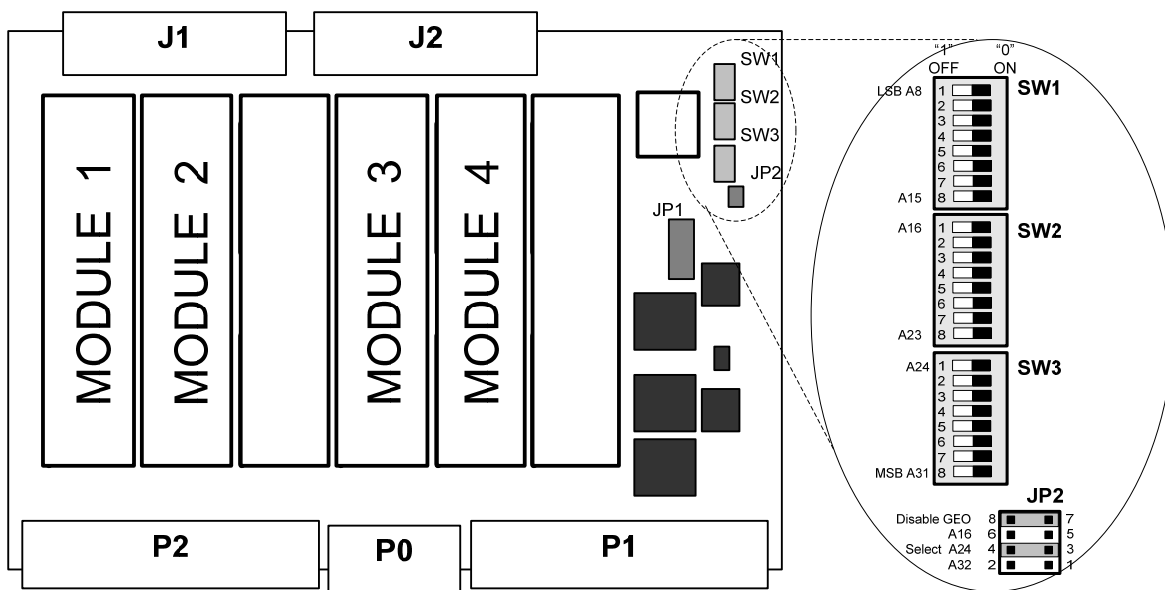
**A16 mode:** Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 256 byte boundaries (Standard), or 512 byte boundaries, when offset addresses above 100 are enabled. See card layout pictorial below. Address switches A8, A9 & A10 are ignored. Card requires 2048 byte boundaries. For detail examples, see 64xxx\_VME\_Board\_Addresssing document on our website <http://www.naii.com>.

Note: Address switch A8 must be set to "ON" (logic 0) for 512 byte boundaries.

**Enable Geographical addressing by removing jumper from JP2.**

**Disable Geographical addressing by adding jumper to JP2.**

See card layout pictorial below. Address switches A8, A9 & A10 are ignored. Card requires 2048 byte boundaries. For detail examples, see 64xxx\_VME\_Board\_Addresssing document on our website <http://www.naii.com>.



**Geographical addressing:** When geographical addressing is enabled the card will respond to address modifier 2FH for A24 address mode, where the 5 Msb's of the A24 address are the 5 bits defined by a slot in VME back plane. The card can optionally be interrogated at 2Fh to determine resource requirement and available functionality. Using the address modifier 2Fh, the following need to be written to the card:

- 1) the base address the card should to respond to
- 2) the address modifier (A16, A24, A32)
- 3) then enable the card

For example : If the card is in slot # 10 the 5 Msb's are 01010 so the address of the CSR registers are : 0101 0 111 1111 1111 xxxx xxxx or 57FFxx h ( xx is CSR register offset)

Write to address 57FF63 h, the A31 – A24 base address bits , for example 01h  
 Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h  
 Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h  
 Write to address 57FF6F h, the address modifier you wish to respond to shifted up 2 bits , e.g. 28h( 0A<< 2 )  
 Then Write to address 57FFBh , 10h to enable the card.

The card will now respond to the base address ( 010204 in the example ) and address modifier ( 0A in example ) programmed. The base address and address modifier can be changed at any time.

### MEMORY MAP

00	Ch.01 Data Hi	R	48	Ratio Ch 10/ Ch 9	R/W	90	Not Used	D8	Velocity, scale Ch.13	R/W	
02	Ch.02 Data Hi	R	4A	Ratio Ch 12/ Ch 11	R/W	92	Not Used	DA	Velocity, scale Ch.14	R/W	
04	Ch.03 Data Hi	R	4C	Ratio Ch 14/ Ch 13	R/W	94	Not Used	DC	Velocity, scale Ch.15	R/W	
06	Ch.04 Data Hi	R	4E	Ratio Ch 16/ Ch 15	R/W	96	Not Used	DE	Velocity, scale Ch.16	R/W	
08	Ch.05 Data Hi	R	50	Angle Δ Ch.01	R/W	98	Not Used	E0	Ch.02 Data Lo	R	
0A	Ch.06 Data Hi	R	52	Angle Δ Ch.02	R/W	9A	Not Used	E2	Ch.04 Data Lo	R	
0C	Ch.07 Data Hi	R	54	Angle Δ Ch.03	R/W	9C	Not Used	E4	Ch.06 Data Lo	R	
0E	Ch.08 Data Hi	R	56	Angle Δ Ch.04	R/W	9E	Not Used	E6	Ch.08 Data Lo	R	
10	Ch.09 Data Hi	R	58	Angle Δ Ch.05	R/W	A0	(A & B) res. Ch.01	R/W	E8	Ch.10 Data Lo	R
12	Ch.10 Data Hi	R	5A	Angle Δ Ch.06	R/W	A2	(A & B) res. Ch.02	R/W	EA	Ch.12 Data Lo	R
14	Ch.11 Data Hi	R	5C	Angle Δ Ch.07	R/W	A4	(A & B) res. Ch.03	R/W	EC	Ch.14 Data Lo	R
16	Ch.12 Data Hi	R	5E	Angle Δ Ch.08	R/W	A6	(A & B) res. Ch.04	R/W	EE	Ch.16 Data Lo	R
18	Ch.13 Data Hi	R	60	Angle Δ Ch.09	R/W	A8	(A & B) res. Ch.05	R/W	F0	Not Used	
1A	Ch.14 Data Hi	R	62	Angle Δ Ch.10	R/W	AA	(A & B) res. Ch.06	R/W	F2	Not Used	
1C	Ch.15 Data Hi	R	64	Angle Δ Ch.11	R/W	AC	(A & B) res. Ch.07	R/W	F4	Not Used	
1E	Ch.16 Data Hi	R	66	Angle Δ Ch.12	R/W	AE	(A & B) res. Ch.08	R/W	F6	Not Used	
20	Velocity Ch.01	R	68	Angle Δ Ch.13	R/W	B0	(A & B) res. Ch.09	R/W	F8	Not Used	
22	Velocity Ch.02	R	6A	Angle Δ Ch.14	R/W	B2	(A & B) res. Ch.10	R/W	FA	Not Used	
24	Velocity Ch.03	R	6C	Angle Δ Ch.15	R/W	B4	(A & B) res. Ch.11	R/W	FC	Not Used	
26	Velocity Ch.04	R	6E	Angle Δ Ch.16	R/W	B6	(A & B) res. Ch.12	R/W	FE	Not Used	
28	Velocity Ch.05	R	70	Angle Δ initiate	R/W	B8	(A & B) res. Ch.13	R/W	100	Ref. Freq.	R/W
2A	Velocity Ch.06	R	72	Active channels,	R/W	BA	(A & B) res. Ch.14	R/W	102	Ref. Voltage	R/W
2C	Velocity Ch.07	R	74	Test (D2) verify	R/W	BC	(A & B) res. Ch.15	R/W	104	Watchdog timer	R/W
2E	Velocity Ch.08	R	76	Test Enable	R/W	BE	(A & B) res. Ch.16	R/W	106	Soft reset	W
30	Velocity Ch.09	R	78	Status, Sig.	R	C0	Velocity, scale Ch.01	R/W	108	Interrupt level	R/W
32	Velocity Ch.10	R	7A	Status, Ref	R	C2	Velocity, scale Ch.02	R/W	10A	Part #	R
34	Velocity Ch.11	R	7C	Status, Test,	R	C4	Velocity, scale Ch.03	R/W	10C	Serial #	R
36	Velocity Ch.12	R	7E	Latch	W	C6	Velocity, scale Ch.04	R/W	10E	Date code	R
38	Velocity Ch.13	R	80	Test angle	W	C8	Velocity, scale Ch.05	R/W	110	Rev Level, PCB	R
3A	Velocity Ch.14	R	82	Angle change alert	R	CA	Velocity, scale Ch.06	R/W	112	Rev Level, Master DSP	R
3C	Velocity Ch.15	R	84	Interrupt Vector , BIT	R/W	CC	Velocity, scale Ch.07	R/W	114	Rev Level, Slave DSP	R
3E	Velocity Ch.16	R	86	Interrupt Vector, Angle Δ	R/W	CE	Velocity, scale Ch.08	R/W	116	Rev Level, Master FPGA	R
40	Ratio Ch 2/ Ch 1	R/W	88	Synchro/Resolver	R/W	D0	Velocity, scale Ch.09	R/W	118	Rev Level, Slave FPGA	R
42	Ratio Ch 4/ Ch 3	R/W	8A	Two Speed Lock-Loss	R	D2	Velocity, scale Ch.10	R/W	11A	Rev Level, VME FPGA	R
44	Ratio Ch 6/ Ch 5	R/W	8C	Not Used		D4	Velocity, scale Ch.11	R/W	11C	Board Ready	R
46	Ratio Ch 8/ Ch 7	R/W	8E	Not Used		D6	Velocity, scale Ch.12	R/W			

## REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data° (Hi) <sup>1</sup>	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Data° (Lo) <sup>1</sup>	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D1
Status, Test	Ch.16	Ch15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.09	Ch.8	Ch.07	Ch.06	Ch.05	Ch.04	Ch.3	Ch.02	Ch.01
Status, Reference	Ch.16	Ch15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.09	Ch.8	Ch.07	Ch.06	Ch.05	Ch.04	Ch.3	Ch.02	Ch.01
Status, Signal	Ch.16	Ch15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.09	Ch.8	Ch.07	Ch.06	Ch.05	Ch.04	Ch.3	Ch.02	Ch.01
Angle change alert	Ch.16	Ch15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.09	Ch.8	Ch.07	Ch.06	Ch.05	Ch.04	Ch.3	Ch.02	Ch.01
Active channels	Ch.16	Ch15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.09	Ch.8	Ch.07	Ch.06	Ch.05	Ch.04	Ch.3	Ch.02	Ch.01
Synchro/Resolver	Ch.16	Ch15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.09	Ch.8	Ch.07	Ch.06	Ch.05	Ch.04	Ch.3	Ch.02	Ch.01
Two Speed Lock-Loss	X	15/16	X	13/14	X	11/12	X	Ch9/10	X	7/8	X	5/6	X	3/4	X	1/2
(A & B) resolution	C/E	X	X	X	X	X	X	X	X	X	X	X	X	D2	D1	D0

	↑		4 pole	16 bit	0	0	0
		“1” = Commutation	6 pole	15 bit	0	0	1
		“0” = Encoder	8 pole	14 bit	0	1	0
			Commutation ↑	13 bit	0	1	1
			or	12 bit	1	0	0
			Encoder outputs ↑				

Note 1 –Values are rounded off

At **Power-ON** or **System Reset**, all parameters are restored to their default values.

**Enter Active Channels:** Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel Register*. “1”=active; “0”=not used. Omitting this step will produce false alarms, because unused channels will set faults.

**Optional Synchro/Resolver Mode:** Where applicable, write a “1” or “0” (Synchro = 1; Resolver = 0) to each bit, representing a channel, of *Synchro/Resolver Register*.

**Ratio:** Enter the desired ratio, as an integer number, in the *Ratio Register* corresponding to the pair of channels to be used for a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

**Read:** For single speed applications (Ratio=1), read individual channels 1,2,3,4,etc. For two-speed applications, read only channels (2,4,6,8,etc.) for the combined output of 16 bits. For resolution up to 24 bits, read Data Hi word, then Data Lo word. Data Hi word, when read, latches low word. Data Low word, when read, unlatches data.

In two-speed S/D applications, the single speed information (coarse) from the synchro should be connected to the odd channel of the pair. The N-speed information (multi-speed, fine) from the synchro should be connected to the even channel of the pair. The pairs are defined as: CH1 & 2, CH3 & 4,... CH15 & 16.

**Two-Speed Lock-Loss:** When two Synchros are geared to each other, either electrically or mechanically, in order to achieve higher accuracy, the misalignment of the Coarse and Fine Synchros must not exceed 90°/gear ratio or the digital angle output may not be valid. Should this problem occur, with a given channel pair, the corresponding bit in the *Two-Speed Lock-Loss Register* will be set to “0”.

**Latch:** Writing the integer 2 to the *Latch Register* will cause all the channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels. Data may also be latched using Hardware Latch control pins 20 & 59 (connectors J1 & J2). Apply 5 volts to latch. Contact Factory Customer Service for hardware latch.

**Velocity Output:** Read Velocity Registers of each channel as a 2’s complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

- When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
- When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
- When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
- When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then

$$\text{Velocity in RPS} = 50.8626 \times \text{E6D5h} / 32,768 = 50.8626 \times -6,442 / 32,768 = -10 \text{ RPS}$$

**Velocity Scale Factor:** The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS)**, where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale Register* for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and -32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor =  $4095(152.5878/152.5878) = 4095 = 0FFFh$ ;  
This results in a velocity resolution of:  $(152.5878 \text{ RPS}/32,767) \times 360^\circ/\text{RPS} = 1.676^\circ/\text{sec}$  (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor =  $4095(152.5878/50.8626) = 12,285 = 2FFDh$ ;  
This is a velocity resolution of:  $(50.8626 \text{ RPS}/32,767) \times 360^\circ/\text{RPS} = 0.5588^\circ/\text{sec}$

For 9.5367 RPS max, Scale Factor =  $4095(152.5878/9.5367) = 65,520 = FFF0h$ ; 0.10477 °/sec resolution (lowest setting)

**D2 Test Enable:** Writing "1" to D2 of *Test Enable Register* initiates automatic background BIT testing that checks each channel every 5° to a test accuracy of 0.05°. An Interrupt (if enabled) will be set to indicate an accuracy problem and the results are available in *Test Status Register* (within 45 sec). A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled. Card will (every 30 seconds) write 55h to Test (D2) Verify register when D2 is enabled. User can periodically clear to Test (D2) Verify register to 0000h and then read again, after 30 seconds, to verify that background BIT testing is activated.

In addition, each S/D Signal and Reference input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and *Reference Status Registers*.

**D3 Test Enable:** Writing "1" to D3 of *Test Enable Register*, initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is not required. Test cycle is completed within 45 seconds and results can be read from the *Test Status Registers*. D3 changes from "1" to "0" when test is complete. A failure will trigger an Interrupt (if enabled). The testing requires no external programming, and can be initiated by writing "1" to D3 or terminated by writing "0" to D3.

Signal and Reference monitoring is disabled during D3 test.

**D0 Test Enable:** Checks card and VME interface. Writing "1" to D0 of *Test Enable Register* disconnects all channels from the outside world, enabling user to write any number of angles to the card at 34h. Data is then read from the VME interface (after writing, allow 400 ms before reading). Test accuracy to be <.05°. Disable by setting D0 to "0". Upon writing "1", the default test angle of D0 is 30°. External reference is not required. (ex.  $330^\circ=1110101010101011$ ).

Signal and Reference monitoring is disabled during D0 test.

**Status, Test:** Check the corresponding bit of the *Test Status Register*, for status of BIT testing for each active channel. A "1" means accuracy passes; A "0" indicates a failure on an active channel. Channels that are inactive are also set to "0" (test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register

**Status, Ref:** Check the corresponding bit of the *Ref Status Register*, for status of the reference input for each active channel. A "1" means Reference ON, a "0" means Reference Loss on active channels. Channels that are inactive are also set to "0" (Reference loss is detected after 2 seconds). Reference monitoring is disabled during D3 or D0 Test. Any Reference status failure, transient or intermittent will latch the *Reference Status Register*. Reading will unlatch register.

**Status, Sig:** Check the corresponding bit of the *Sig Status Register*, for status of the input signals for each active channel. A "1" means Signal is valid (level must be a minimum of 2V), a "0" means Signal loss on active channels. (Signal loss is detected after 2 seconds). Channels that are inactive are also set to "0". Signal monitoring is disabled during D3 and D0 test. Any Signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.

**Interrupt Priority:** Enter requirements as a 16-bit integer. 0 = no interrupt; 1-7 indicates priority levels. Any error will latch Status Register and trigger an Interrupt. When Interrupt is acknowledged, additional errors will set another Interrupt. Reading will unlatch registers. Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. Within 250ms registers will be updated with the background data. Allow 250 ms to scan all channels.

**Interrupt Vector, BIT:** Write 16-bit integer (0-255). Used for failure reports.

**Interrupt Vector, Angle Δ:** Write 16-bit integer (0-255). Used for angle change alert reports.

**Angle Change Alert:** Write a 16-bit word to each channel, to represent the minimum differential required. MSB=180°; minimum differential is 0.05°. Setting to zero disables the Angle Change Alert for a given channel. Initiate monitoring

by writing "1" to Angle Change Initiate Register. When that differential is exceeded, on any monitored channel, an interrupt is generated. Read Angle Change Alert Flag Register at 96h for status of each channel ("0" = no change, "1" = change)

**Soft Reset:** (Level sensitive): Writing a "1" initiates and holds software in reset state. Then, writing "0" initiates reboot (takes 400 ms). Status Registers cleared; Watchdog Timer functional; Failure bit at "0"; Angle outputs held at last update; Interrupts disabled.

**Watchdog Timer:** This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. User, after 100 µSec, should look for the inverted code to confirm that the processor is operating.

**Optional Reference Supply:** For frequency, write a 16-bit word (Ex: 400 Hz = 1 1001 0000) to address 100. For voltage, write a word (Ex: 26.1 Vrms =1 0000 0101) with LSB=0.1 Vrms, to address 102. It is recommended that user program the required frequency before setting the output voltage

**Optional (A&B) Encoder or Commutation (A,B,C):** Enter required Encoder resolution, for each channel, per above table or set the required motor poles (see Register Bit Map). Can be changed on the fly. The MSB sets the channel for either Encoder or Commutation. Default is 12-bit encoder mode.

**Part Number:** Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

**Serial Number:** is read as a 16-bit binary word. A unique 16 bit code is assigned to each model number.

**Date Code:** Read as a decimal number. The four digits represent YYWW (Year,Year,Week,Week)

**Revisions:** Read as a 16-bit binary word.

**Board Ready:** Poll register. Board is ready to be accessed **only after** you read "AA55". (within 1 second after board power-on)

**Front panel Connectors: J1 & J2:** AMP 748483-5 Mate: AMP 748368-1

J1			
Pin	Slot 1	Pin	Slot 2
1	S1-CH1	27	S1-CH5
21	S3-CH1	8	S3-CH5
2	S2-CH1	28	S2-CH5
22	S4-CH1	9	S4-CH5
3	RHI-CH1	29	RHI-CH5
23	RLO-CH1	10	RLO-CH5
4	S1-CH2	30	S1-CH6
24	S3-CH2	11	S3-CH6
5	S2-CH2	31	S2-CH6
25	S4-CH2	12	S4-CH6
6	RHI-CH2	32	RHI-CH6
26	RLO-CH2	13	RLO-CH6
40	S1-CH3	66	S1-CH7
60	S3-CH3	47	S3-CH7
41	S2-CH3	67	S2-CH7
61	S4-CH3	48	S4-CH7
42	RHI-CH3	68	RHI-CH7
62	RLO-CH3	49	RLO-CH7
43	S1-CH4	69	S1-CH8
63	S3-CH4	50	S3-CH8
44	S2-CH4	70	S2-CH8
64	S4-CH4	51	S4-CH8
45	RHI-CH4	71	RHI-CH8
65	RLO-CH4	52	RLO-CH8
20	Latch Lo <sup>1</sup>	59	Latch Hi <sup>1</sup>

J2			
Pin	Slot 4	Pin	Slot 5
1	S1-CH9	27	S1-CH13
21	S3-CH9	8	S3-CH13
2	S2-CH9	28	S2-CH13
22	S4-CH9	9	S4-CH13
3	RHI-CH9	29	RHI-CH13
23	RLO-CH9	10	RLO-CH13
4	S1-CH10	30	S1-CH14
24	S3-CH10	11	S3-CH14
5	S2-CH10	31	S2-CH14
25	S4-CH10	12	S4-CH14
6	RHI-CH10	32	RHI-CH14
26	RLO-CH10	13	RLO-CH14
40	S1-CH11	66	S1-CH15
60	S3-CH11	47	S3-CH15
41	S2-CH11	67	S2-CH15
61	S4-CH11	48	S4-CH15
42	RHI-CH11	68	RHI-CH15
62	RLO-CH11	49	RLO-CH15
43	S1-CH12	69	S1-CH16
63	S3-CH12	50	S3-CH16
44	S2-CH12	70	S2-CH16
64	S4-CH12	51	S4-CH16
45	RHI-CH12	71	RHI-CH16
65	RLO-CH12	52	RLO-CH16
72	RLO out	33	RHI out
20	Latch Lo <sup>1</sup>	59	Latch Hi <sup>1</sup>

Note 1: Contact Factory Customer Service

## P2 Connector: (Always Active)

Pin	Ch.	Pin	Ch.	Pin	Ch.	Pin	Ch.
25a	S1-CH1	12a	S1-CH5	16c	S1-CH9	7a	S1-CH13
26a	S3-CH1	13a	S3-CH5	17c	S3-CH9	7c	S3-CH13
27a	S2-CH1	14a	S2-CH5	18c	S2-CH9	22a	S2-CH13
28a	S4-CH1	15a	S4-CH5	19c	S4-CH9	22c	S4-CH13
29a	RHI-CH1	16a	RHI-CH5	20c	RHI-CH9	1d	RHI-CH13
30a	RLO-CH1	17a	RLO-CH5	21c	RLO-CH9	2d	RLO-CH13
31a	S1-CH2	18a	S1-CH6	23c	S1-CH10	3d	S1-CH14
32a	S3-CH2	19a	S3-CH6	24c	S3-CH10	4d	S3-CH14
25c	S2-CH2	20a	S2-CH6	1a	S2-CH10	5d	S2-CH14
26c	S4-CH2	21a	S4-CH6	2a	S4-CH10	6d	S4-CH14
17d	RHI-CH2	21d	RHI-CH6	25d	RHI-CH10	29d	RHI-CH14
18d	RLO-CH2	22d	RLO-CH6	26d	RLO-CH10	30d	RLO-CH14
27c	S1-CH3	23a	S1-CH7	3a	S1-CH11	7d	S1-CH15
28c	S3-CH3	24a	S3-CH7	4a	S3-CH11	8d	S3-CH15
29c	S2-CH3	8c	S2-CH7	5a	S2-CH11	9d	S2-CH15
30c	S4-CH3	9c	S4-CH7	6a	S4-CH11	10d	S4-CH15
31c	RHI-CH3	10c	RHI-CH7	1c	RHI-CH11	11d	RHI-CH15
32c	RLO-CH3	11c	RLO-CH7	2c	RLO-CH11	12d	RLO-CH15
8a	S1-CH4	12c	S1-CH8	3c	S1-CH12	13d	S1-CH16
9a	S3-CH4	13c	S3-CH8	4c	S3-CH12	14d	S3-CH16
10a	S2-CH4	14c	S2-CH8	5c	S2-CH12	15d	S2-CH16
11a	S4-CH4	15c	S4-CH8	6c	S4-CH12	16d	S4-CH16
19d	RHI-CH4	23d	RHI-CH8	27d	RHI-CH12	29z	RHI-CH16
20d	RLO-CH4	24d	RLO-CH8	28d	RLO-CH12	31z	RLO-CH16
		25z	RHI-OUT			27z	RLO-OUT

**Notes: On P2 row z, all even numbered pins are grounded**  
DO NOT CONNECT TO ANY UNDESIGNATED PINS

## Encoder/Commutation Output Connections

P0 Connector : except IDXHI-CH16 & IDXLO-CH16 are on P2

Pin	Ch.	Pin	Ch.	Pin	Ch.	Pin	Ch.
B8	AHI-CH1	B14	AHI-CH5	A1	AHI-CH9	C5	AHI-CH13
C8	ALO-CH1	C14	ALO-CH5	A2	ALO-CH9	A6	ALO-CH13
D8	BHI-CH1	D14	BHI-CH5	A3	BHI-CH9	B6	BHI-CH13
E8	BLO-CH1	E14	BLO-CH5	A4	BLO-CH9	C6	BLO-CH13
E9	IDXHI-CH1	E15	IDXHI-CH5	A5	IDXHI-CH9	D6	IDXHI-CH13
D9	IDXLO-CH1	D15	IDXLO-CH5	B5	IDXLO-CH9	E6	IDXLO-CH13
C9	AHI-CH2	C15	AHI-CH6	B1	AHI-CH10	E7	AHI-CH14
B9	ALO-CH2	B15	ALO-CH6	B2	ALO-CH10	D7	ALO-CH14
B10	BHI-CH2	B16	BHI-CH6	B3	BHI-CH10	C7	BHI-CH14
C10	BLO-CH2	C16	BLO-CH6	B4	BLO-CH10	B7	BLO-CH14
D10	IDXHI-CH2	D16	IDXHI-CH6	C1	IDXHI-CH10	A7	IDXHI-CH14
E10	IDXLO-CH2	E16	IDXLO-CH6	C2	IDXLO-CH10	A8	IDXLO-CH14
E11	AHI-CH3	E17	AHI-CH7	D1	AHI-CH11	A9	AHI-CH15
D11	ALO-CH3	D17	ALO-CH7	D2	ALO-CH11	A10	ALO-CH15
C11	BHI-CH3	C17	BHI-CH7	D3	BHI-CH11	A11	BHI-CH15
B11	BLO-CH3	B17	BLO-CH7	D4	BLO-CH11	A12	BLO-CH15
B12	IDXHI-CH3	B18	IDXHI-CH7	D5	IDXHI-CH11	A13	IDXHI-CH15
C12	IDXLO-CH3	C18	IDXLO-CH7	E5	IDXLO-CH11	A14	IDXLO-CH15
D12	AHI-CH4	D18	AHI-CH8	E1	AHI-CH12	A15	AHI-CH16
E12	ALO-CH4	E18	ALO-CH8	E2	ALO-CH12	A16	ALO-CH16
E13	BHI-CH4	E19	BHI-CH8	E3	BHI-CH12	A17	BHI-CH16
D13	BLO-CH4	D19	BLO-CH8	E4	BLO-CH12	A18	BLO-CH16
C13	IDXHI-CH4	C19	IDXHI-CH8	C4	IDXHI-CH12	P2.1z	IDXHI-CH16
B13	IDXLO-CH4	B19	IDXLO-CH8	C3	IDXLO-CH12	P2.3z	IDXLO-CH16

**NOTE:** For commutation (A,B,C) outputs: A Hi becomes A, B Hi becomes B, and Index Hi becomes C.

## Code Table

Code	Input (VL-L)	Ref (Vrms)	Frequency (Hz)	Notes
01	11.8	26	400	
02	90	115	400	
03	90	115	50/400	
04	2-26	2-26	400	
05	2-26	2-26	800	
06	2-26	2-26	1000	
07	2-26	2-26	1200	
08	2-26	2-26	1600	
09	2-26	2-26	2000	
10	2-26	2-26	2500	
11	2-26	2-26	3000	
12	2-26	2-26	4000	
13	2-26	2-26	5000	
14	2-26	2-26	6500	
15	2-26	2-26	7000	
16	2-26	2-26	10000	
17	2-26	115	400	

See code list addendum for descriptions of code 50 and above.

**IMPORTANT: Tracking rate and bandwidth can easily be customized to meet your specific requirements.**

## PART NUMBER DESIGNATION

**64SD3- XX X X X X - XX**

### TOTAL NUMBER OF CHANNELS(\*)

04 – 4 S/D Channels  
 08 – 8 S/D Channels  
 12 – 12 S/D Channels  
 16 – 16 S/D Channels

### ENVIRONMENTAL

C = 0°C to +70°C  
 E = -40°C to +85°C  
 H = E With Removable Conformal Coating  
 K = C With Removable Conformal Coating  
 contact factory for other temperature requirements

### FORMAT

S = Synchro  
 R = Resolver  
 M = Mixed (See Code Table)  
 P = Synchro/Resolver Programmable

CODE (See Code Table)

### OPTIONAL REFERENCE SELECTION

### ENCODER/COMMUTATION

- = Without Encoder/Commutation option  
 E = With Encoder/Commutation option  
 (Adds P0 Connector)

### OPTIONAL REFERENCE SELECTION

0 = No "On Board Reference"  
 A = 2-28 VRMS output  
 C = 115 VRMS fixed output

### MECHANICAL

F = Front Panel I/O and P2 I/O  
 P = P2 I/O only  
 W = P With Wedgelocks  
 A = VME64 with Blank Front Panel and P2 I/O only  
 B = VME64 Front Panel unshielded\*\*\*  
 with Front Panel I/O & P2 I/O  
 D = VME64 with Blank Front Panel, Low profile  
 extractors and P2 I/O only

## NOTE:

\*\*\* Unshielded to accommodate for mating 78 pin connector.

## Revision Page

Revision	Description of Change	Engineer	Date
1	Initial Release	FH	04/08/02
2	Made 24 bit combined resolution as standard	FH	04/27/02
2.1	Corrected PN (to ABC coding). Updated Max Vel. Data to 152.5878 rps. Added Synchro/Resolver Register	GS	05/30/02
2.2	Added Board Ready Reg description. Read "AA55" when bd is ready within 1s. Removed POST reference in Feature section	GS	06/07/02
2.3	Removed 2-13.5 volt reference option (from spec, and PN)	GS	6/28/02
2.4	Standardized PN, Mech Options List to FPWABD. Mechanical Option B is unshielded to accommodate 78 pin mating connector.	GS	7/30/02
2.5	Added Encoder Pin out (P0)	GS	10/7/2
2.6	Removed "saved parameters remain saved from Soft Reset:	GS	11/19/02
2.7	Added J1 & J2 pins 20-, 59+ HARDWARE LATCH and its description incl contact factory. Revealed Revision Control Page. Showed D15 Commutation/Enc bit in A&B res reg	GS	1/24/03
2.8	Added Codes 4-17	GS	2/26//3
2.9	Added Dip Switch Pictorial	GS	12/22/3
3.0	Change Layout Dwg to include modules 1-4 (not 1-6)	GS	2/19/4
3.1	Opt Ref Supply programming is at address 100 and 102 (not 3A and 3C)	GS	3/8/4
3.2	Order option E adds P0 connector	GS	3/24/4
3.3	FOR COMMERCIAL AND MILITARY APPLICATIONS. If enabled, D2 Test Enable will write 55h to Test (D2) Verify register approximately every 30s.	GS	3/17/5
3.4	New Address	KL	4/25/07

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