Model VME-64SW2

HIGH CURRENT DRIVE

VMEbus
THIRTY-TWO (32) 2 AMP. ISOLATED HIGH CURRENT DRIVERS
High-side Switched
Opto-isolated**,** wrap-around self test

FEATURES:

- Short circuit protected
- 32 channels in two groups of 16 each
- Soft turn-on and turn-off
- Watchdog timer and soft reset
- Conforms to ANSI/VITA 1.1-1997 VME64 extension
- Conforms to VITA 1.-1994
- ESD protected to IEC 1000-4 Level 2
- Sense unconnected loads
- Geographical addressing
- Part number, S/N, Date code, & Rev. in non-volatile memory

DESCRIPTION:

This single slot card, incorporates 32 high-side switched outputs with short circuit protection and extensive diagnostics. Wrap-around testing continuously monitors each channel for short circuit, unconnected loads, missing loads and for shorted channels. Any failure will trigger an Interrupt, within 5 seconds of channel diagnostic completion. If the 28 VDC power fails and even if VME power fails at the same time, and even if all channels have 2 A, 2 Henry loads connected, the card is fail proof and will provide for the safe discharge of all inductive loads. Both input voltages are continuously monitored and the actual measured voltages can be read from registers.

The card is divided into two groups of 16 channels that can be independently powered up or down. VME interface power is opto-isolated from the switched external power.

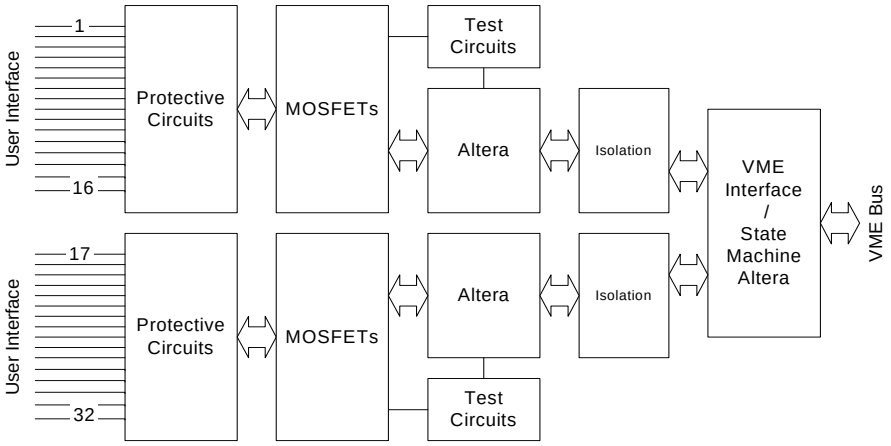
Current interruption transient protection, for inductive loads, is incorporated for each channel. When the loads are resistive and drawing 2 amperes, the total steady state summed driver channel power dissipated by the board is 8.7 watts. As the loads become more inductive, the dynamic driver channel power dissipation increases based on inductance, current, and duty cycle, and care has to be taken to prevent the total summed driver channel dynamic power dissipation from exceeding 40 watts. A 2Henry, 2A inductive load, when driven at a 1 Hz rate, will result in a dynamic driver channel power dissipation of 3.6 watts. For ease of calculation, reducing the inductance, current or duty cycle will decrease the power dissipation linearly and increasing the inductance, current or duty cycle will increase the power dissipation linearly. Thus, reducing the rep. rate from 1 to 1/3 will decrease the dynamic driver channel power dissipation to 1.2 watts. The max repetition rate depends on how quickly the stored energy can be discharged. Special circuitry incorporated in our design clamps the discharge voltage at -80 volts (when 28 VDC power is applied) thus assuring a fast drop out time. (actual drop-out time depends on inductance and current). Therefore, drop out time for a 2Hy solenoid operating at 28 VDC and drawing 2A is 42 ms. Drop out time for a 1Hy solenoid operating at 28 VDC and drawing 1A is 10 ms.

Use of power MOSFET switching devices, substantially reduces power consumption and therefore heat generated. **If higher current drive is required, two or more outputs can be connected in parallel.** Soft turn-on and turn-off is incorporated to minimize high frequency noise generation. Two watchdog timers monitor communication across the opto-isolators (one for each group of 16). A signal loss (BIT polling) of 1 second will cause that group of 16 to be turned OFF and set a “Failure” register to “0”. A soft reset is required to reset the Failure bit. A ‘Board Ready’ register is provided that indicates when the card is ready to be accessed. To simplify logistics, Part number, S/N, Date code, & Rev. are located in non-volatile memory locations. All “E” cards are cycled from -40°C to +85°C for 24 hours.

SAFETY FEATURES:

1. Any output is Deenergized (OPEN) if a steady state current of 2.5 A to 5.0 A is sensed for 60 ms. The output will remain OPEN until reset by an OVERLOAD RESET command.
2. Power "On" will latch all Data Write lines at "0" (Loads deenergized) until card is addressed.
3. Loss of VME power will cause all loads to be OPENED.
4. Four separate registers are supplied to monitor loads. One will indicate if an external load is connected, another will indicate if a particular channel was automatically shut down by an overload condition, another register will indicate the commanded Energized/Deenergized condition of each channel, and the fourth register will indicate if a channel that is commanded OPEN is actually SHORTED.
5. Two watchdog timers sense communication between the switch drivers and the processor across the opto-isolators (one for each group of 16). A signal loss (BIT polling) of 1 second will cause that group of 16 to be turned OFF and will also set a "Failure" register to "0". A soft reset is required to reset the Failure bit.
6. No power sequencing is required.
7. If a channel is sensed to be SHORTED when commanded to be OPEN, an interrupt will be set.

Relay Driver Block Diagram



SPECIFICATIONS:

Number of Channels:	32 Opto-isolated channels in two groups of 16 each
Drive Voltage:	+5 VDC min.; 28 VDC Nominal; +40 VDC max.
Drive capability:	2.0 A resistive. Continuous to +85°C (dissipates 0.27 w/ channel). 2.0 A into 2 Hy at a 1 Hz rate. Continuous to +85°C (dissipates 1.20 w/ channel). 1.8 A into 1 Hy at a 1 Hz rate. Continuous to +85°C (dissipates 1.20 w/ channel). Power dissipation increases with rate and/or inductance. (See description)
Over-current conditions:	Hardware limits any short circuit to 25A at +25°C or 20A at +85°C. After 3 ms.. software then shuts down that channel. Software will also shut down a channel under the following conditions: A steady state current between 2.5 to 5 amperes after 60 milliseconds An inrush current above 5 amperes after 3 milliseconds
Reverse current capability:	Each channel can safely discharge the reverse current generated by inductive loads of up to 2 Hy at 2 A. Reverse current circuitry will hold the drive at Vcc-110 volts for 42 milliseconds at 2 Hy and 2 A. Lower inductance or lower current will decrease the drop-out time. **Note:** With +28 VDC input, the discharge voltage is clamped at –80 VDC. At +5VDC the clamping voltage will be about –105VDC.
Leakage current:	160 μa max. at +85° C and +40 VDC
ON resistance:	0.05 Ω nominal, 0.068 Ω max.
Rise time:	20μs min. 100μs nominal (driving a 2.0 A resistive load)
Fall time:	20μs min. 50μs nominal (driving a 2.0 A resistive load)
Protection:	Each channel incorporates current interruption transient protection and is also protected against 250 V transients (600 mjoules for 0.05ms)
ESD protection:	Designed to meet the testing requirements of IEC 1000-4 Level 2. (8KV transient with a peak current of 30 A)
Power:	+5 VDC at 0.75A
Power dissipation:	With an 85°C board edge temperature, no component junction temperature will exceed 105°C under worst case operating condition.

Isolation from VMEbus:	250 VAC (350 VDC)
Open circuit sense:	If a channel is commanded to energize and the load current drops below 40ma, card will set a “load missing” flag (if enabled).
Base address:	Responds to geographical addressing.
Interrupts:	One Interrupt capability is implemented. One of seven priority lines can be specified.
VME Data transfer:	**Data transfers within 200 ns**
Temperature, operating:	-40°C to +85°C
Storage temperature:	-55°C to +105°C
Size:	6U (9.2") height, 4HP (0.8") width. 233.4 mm x 20.3 mm x 160 mm deep
Weight:	24 oz.

PROGRAMMING INSTRUCTIONS

I/O Configuration: The VMEbus interface will automatically respond to A32:D16, A24:D16 and A16:D16 DTB cycles.
A32 mode: Responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 256 byte boundaries.
A24 mode: Unit responds to address modifiers 3A, 3D, 3E and 39. The base address can be anywhere in the 16 Megabyte address space on 256 byte boundaries.
A16 mode: Unit responds to address modifiers 2A, 2D, 2E and 29. The base address can be anywhere in the 64 K byte address space on 256 byte boundaries.
Enable Geographical Addressing by removing jumper from JP2. Disable Geographical Addressing by adding jumper to JP2.

Geographical Addressing: When Geographical Addressing is enabled, the card will respond to address modifier 2Fh for A24 Address mode, where the 5 MSBs of the A24 address are the 5 bits defined by the slot in VME back plane. The Card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using the address modifier 2Fh, the following need to be written to the card:
1) the base address the card should to respond to
2) the address modifier (A16, A24, A32)
3) then enable the card.

For example : If the card is in slot # 10 the 5 Msb’s are 01010 so the address of the CSR registers are :
0101 0 111 1111 1111 xxxx xxxx or 57FFxx h (xx is CSR register offset)
Write to address 57FF63 h, the A31 – A24 base address bits , for example 01h
Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h
Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h
Write to address 57FF6F h the address modifier you wish to respond to shifted up 2 bits, for example 28h (03A << 2)
Then Write to address 57FFFBh , 10h to enable the card.
The card will now respond to the base address (010204 in the example) and address modifier (0A in example) programmed. The base address and address modifier can be changed at any time.

MEMORY MAP

02	Ch.01-16 (Control)	R/W	1A	Interrupt vector 2 (Load missing)	R/W	32	Rev level, PCB	R
04	Ch.17-32 (Control)	R/W	1C	Watchdog timer (communication 01-16)	R	34	Part #	R
06	Ch.01-16 (Short circuit)	R	1E	Watchdog timer (communication 17-32)	R	36	Board Ready	R
08	Ch.17-32 (Short circuit)	R	20	Watchdog timer (μP)	R/W	38	Channels shorted 01-16	R
0A	Ch.01-16 (Load missing)	R	24	Soft reset	W	3A	Channels shorted 17-32	R
0C	Ch.17-32 (Load missing)	R	26	+VDC-A	R	3C	Interrupt mask, Shorted Ch. 01-16	R/W
0E	Interrupt mask, Load missing 01-16	R/W	28	+VDC-B	R	3E	Interrupt mask, Shorted Ch. 17-32	R/W
10	Interrupt mask, Load missing 17-32	R/W	2A	Overload Reset 01-16	W	40	Interrupt vector 3 (shorted channel)	R/W
12	Interrupt mask, Short circuit 01-16	R/W	2C	Overload Reset 17-32	W	42	Rev. Level, Processor	R
14	Interrupt mask, Short circuit 17-32	R/W	2E	Serial number	R	44	Rev. Level, FPGA	R
16	Interrupt level	R/W	30	Date code	R			
18	Interrupt vector 1 (short circuit)	R/W	32	Rev level, PCB	R			

REGISTER BIT MAP

		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Control	01-16	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08	Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01
Control	17-32	Ch32	Ch31	Ch30	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
Overload	01-16	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08	Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01
Overload	17-32	Ch32	Ch31	Ch30	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
Load missing	01-16	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08	Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01
Load missing	17-32	Ch32	Ch31	Ch30	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
Interrupt mask, Load missing	01-16	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08	Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01
Interrupt mask, Load missing	17-32	Ch32	Ch31	Ch30	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
Interrupt mask, Overload	01-16	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08	Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01
Interrupt mask, Overload	17-32	Ch32	Ch31	Ch30	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
Interrupt mask, Shorted Ch.	01-16	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08	Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01
Interrupt mask, Shorted Ch.	17-32	Ch32	Ch31	Ch30	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
Shorted channels	01-16	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08	Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01
Shorted channels	17-32	Ch32	Ch31	Ch30	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
Overload Reset	01-16	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08	Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01
Overload Reset	17-32	Ch32	Ch31	Ch30	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17

STATUS:

Control:	"0" = Load Deenergized. (Open)	"1" = Load Energized (Closed
Short circuit:	"0" = Channel overloaded	"1" = Channel normal.
Loads connected	"0" = Load missing	"1" = Load connected
Interrupt mask:	"0" = Interrupt Disabled.	"1" = Interrupt Enabled
Interrupt mask, Shorted Ch.	"0" = Channel short	"1" = Normal
Overload Reset:	"0" = No change	"1" = Reset Overload shutdown flip-flop

Watchdog timer (Communication failure): See description below

Power ON will latch all Data Write lines at "0" (Loads Deenergized) until card is addressed. All parameters are restored to their default condition..

Enter Interrupt level into address 16h as a 16 bit binary number. 0= no interrupt; 1-7 indicates priority levels. Any error will latch status register and trigger an Interrupt. When Interrupt is acknowledged, additional errors will set another Interrupt. Reading will unlatch registers. Now, consider what happens when a status bit changes before registers are read. For example, if a load loss was detected and latched into registers and subsequent scans find that the load was reconnected, then this status change will be held in background until registers are read. Within 250 ms registers will be updated with the background data. Allow 250 ms to scan all channels.

Board Ready: Poll 36h. Board is ready to be accessed **only after** you read "AA55h " at 36h.

Automatic background bit testing for overload and/or disconnected output is always functional. User can either set an Interrupt to indicate any failure or can poll the registers.

Drive Voltage (26h & 28h): Read actual applied voltage. LSB=100mV. Ex: 27.1 VDC=10Fh;

Interrupt Vector 1 (Short circuit): Write 8 bit word (1-255)

Interrupt Vector 2 (Load missing): Write 8 bit word (1-255)

Interrupt Vector 3 (Channel shorted): Write 8 bit word (1-255)

Overload Reset: Write "1" to 2A/2C to reset any channel that was shut down by an overload. A channel turned OFF by an overload condition cannot be reset by the control registers 02h/04h

Watchdog timer (Communication failure): Two watchdog timers monitor communication between the switch drivers and the processor across the opto-isolators (one for each group of 16). A Signal loss, Bit polling of 1second, will turn OFF that group of 16 and set D0 of register 1Ch and/or 1Eh to "0". A soft reset is required to reset.

Watchdog timer (μP): This feature monitors the watchdog timer register (20h). When it detects that a code has been received, that code will be inverted within 100 μSec. The inverted code stays in the register until replaced by a new code. User, after 100 μSec. should look for the inverted code to confirm that the processor is operating.

Soft reset (Level sensitive): "1" to 24h initiates and holds software reset state. Then, writing "0" initiates reboot (takes 400 ms). This function is equivalent to a power-on reset.

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned for each part number.

Serial Number and Rev's: Read as a 16 bit binary word.

Date Code: Read as a decimal number at 30h. The four digits represent YYWW (Year,Year,Week.Week)

P3 AirBorn Inc. WTB40PR7SY

Pin		Pin		Pin	
1	Output Ch1	15	Output Ch11	29	+VDC-A
2	Output Ch2	16	Output Ch12	30	+VDC-A
3	Output Ch3	17	Output Ch13	31	+VDC-A
4	Output Ch4	18	Output Ch14	32	+VDC-A
5	Output Ch5	19	Output Ch15	33	+VDC-A
6	Output Ch6	20	Output Ch16	34	+VDC-A
7	Output Ch7	21	VDC return-A	35	+VDC-A
8	Output Ch8	22	VDC return-A	36	VDC return-A
9	+VDC-A	23	VDC return-A	37	VDC return-A
10	+VDC-A	24	VDC return-A	38	VDC return-A
11	+VDC-A	25	VDC return-A	39	VDC return-A
12	+VDC-A	26	+VDC-A	40	VDC return-A
13	Output Ch9	27	+VDC-A		
14	Output Ch10	28	+VDC-A		

P4 AirBorn Inc. WTB40PR7SY

Pin		Pin		Pin	
1	Output Ch17	15	Output Ch27	29	+VDC-B
2	Output Ch18	16	Output Ch28	30	+VDC-B
3	Output Ch19	17	Output Ch29	31	+VDC-B
4	Output Ch20	18	Output Ch30	32	+VDC-B
5	Output Ch21	19	Output Ch31	33	+VDC-B
6	Output Ch22	20	Output Ch32	34	+VDC-B
7	Output Ch23	21	VDC return-B	35	+VDC-B
8	Output Ch24	22	VDC return-B	36	VDC return-B
9	+VDC-B	23	VDC return-B	37	VDC return-B
10	+VDC-B	24	VDC return-B	38	VDC return-B
11	+VDC-B	25	VDC return-B	39	VDC return-B
12	+VDC-B	26	+VDC-B	40	VDC return-B
13	Output Ch25	27	+VDC-B		
14	Output Ch26	28	+VDC-B		

NOTE: P2 connector is used only for A32 interface.
Mating connectors are not supplied

PART NUMBER DESCRIPTION

64SW2–32 * *

MECHANICAL:
F = Front Panel I/O
A = VME64 Front Panel, with Front Panel I/O only, standard VME64 extractors
L= VME64 Front Panel, with Front Panel I/O and with low profile extractors

ENVIRONMENTAL:
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating