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# *APU-FDX-2*

**USB Module for**
**AFDX/ ARINC664**
**Test & Simulation**


Avionics Databus Solutions

# APU-FDX-2

*USB Module for AFDX/ ARINC664 Test & Simulation*

product guide

## General Features

The APU-FDX-2 offers full function test, simulation, monitoring and analyser functions for AFDX/ ARINC664 (Avionics Full Duplex Switched Ethernet) networks. It's unique onboard processing capability, memory resources, powerful and customised AFDX/ ARINC664 MACs and IRIG-B time encoder/ decoder gives AFDX/ ARINC664 users features for the most demanding AFDX/ ARINC664 applications.

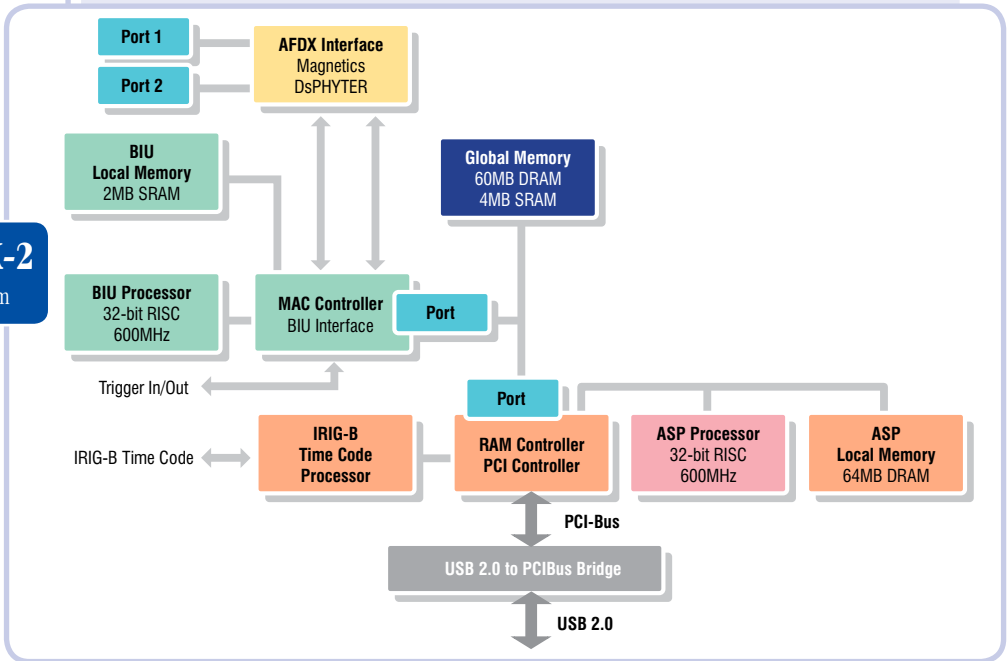
APU-FDX-2 modules are powered from the host computer via the USB connection - no external power adapter is required. Designed in a shirt-pocket sized box the APU-FDX-2 USB module provides two AFDX /ARINC664 ports being configured as two single or one dual redundant port each implementing a 10/100MBit full duplex Ethernet interface. Ports can operate concurrently in traffic simulator and receiver/ monitor modes with support for AFDX/ ARINC664 port related frame statistics. Virtual Link (VL) packet capturing and monitoring features are complimented with powerful triggering and filtering capabilities. The APU-FDX-2 uses AIM's field proven 'Common Core' hardware design utilising two advanced RISC processors, one acting as Bus Interface Unit Processor and one as Application Support Processor (ASP). The vast memory resources allow to implement large receive buffers and complex transmit scenarios onboard. An AFDX/ ARINC664 specific Physical Bus Interface implements two full duplex ports for connection to AFDX/ ARINC664 networks.

A common Application Programming Interface (API) supports all AIM AFDX/ ARINC664 modules.

Full function driver software is delivered with the APU-FDX-2 boards in comprehensive Board Software Packages (BSP's) for different operating systems. The optional PBA.pro™ Databus Test & Analysis Tool (for Windows & Linux) and fdXplorer/ ParaView Data Network Analyser/ Visualiser Software (for Windows) can also be purchased for use with APU-FDX-2 modules.

- *Two advanced 600 MHz XSCALE Processors onboard*
- *Designed for Applications such as:*
  - *Test & Verification of 'End Systems'*
  - *'Switch' Testing*
  - *Monitoring of Traffic between 'End Systems' & 'Switch'*
  - *Inter Switch Traffic Analysis*
  - *Multi Stream High Level System Integration*
- *Programmable Ports - Traffic Simulator and Receiver/ Monitor concurrently*
- *Synchronised Timing across Multiple Modules*
- *Driver Software for WindowsXP/Vista/7, Linux*

**APU-FDX-2**
Block Diagram



## Key Features

- *Robust and Low Power USB2.0 Module*
- *Powered via USB, no external Power Adapter required*
- *Hot plug Capability*
- *Two full duplex AFDX/ ARINC664 Ports configurable to one dual-redundant AFDX/ ARINC664 Port*
- *Programmable Ports - Traffic Simulator and Receiver/ Monitor concurrently*
- *Full Error Injection/ Detection Capability*
- *Multi Level Triggering for Capturing/ Filtering*
- *Real Time Recording and synchronised Bus Replay*
- *Onboard Time Tagging*
- *Drivers for WindowsXP/Vista/7, LabVIEW VI's, Linux*
- *Compatible with **PBA.pro**™ Databus Test & Analysis Tool (for Windows and Linux) and **fdXplorer**/ **ParaView** Network Analyser/ Visualiser Software (for Windows)*
- *Compatible with AIM's **EasyLOAD-615A** Dataloader Software (for Windows)*
- *Software compatible with AIM's family of PMC, PCI, PC-Card, CompactPCI and VME AFDX/ ARINC664 Cards*

## Traffic Generation

The APU-FDX-2 provides real time traffic generation on both ports concurrently. Transmitter operation allows users to fully programme all fields of the AFDX/ ARINC664 frame including the Virtual Link identifier, MAC source address, IP structure, UDP structure, payload and sequence number. Multiple modes of transmit sequencing are supported, these being Generic/ Replay and UDP port oriented shaped transmissions. Users can programme payload data with user defined or fixed data. Inserting the time tag in the payload data provides an elegant solution to measure frame transmit delays through the network. Synchronisation of transmissions across multiple ports is achieved by using strobe Inputs/ Outputs.

- *Programmable Timing & Sequencing of Frames*
- *Physical Error Injection - CRC, Gap, Size, Alignment*
- *Logical Error Injection on Layers 2, 3, 4*
- *Timing Error Injection - Violation of Bandwidth Allocation Gap (BAG)*
- *Autonomous Dynamic Data Generation*
- *UDP Port Simulation with Traffic Shaping & Sequence Numbering*
- *Support for Sampling and Queuing Ports*

## UDP/VL Receive Mode

The APU-FDX-2 module ports can be configured to work in UDP/ VL oriented receive mode. In this mode each UDP port has a separate buffer queue. Received frames are stored with frame headers containing time tag and status information. Frame header information can be stored and payload data optionally discarded for the testing of switches and the complete network. With the traffic shaping verification enabled, any violations are reported as errors in related frame headers.

- *VL oriented Filtering*
- *Second Level Filtering on Generic Frame Parameter*
- *Time Stamping of Received Packets with extended IRIG-B Time Code (1µs)*
- *Physical Error Detection, Frame Level - CRC, Gap, Size and Alignment*
- *AFDX/ ARINC664 Specific Error Detection*
  - *Traffic Shaping Verification*
  - *Verification of MAC, IP and UDP Headers*
  - *VL oriented Integrity Checking*

## Chronological Receive Mode

(Monitor Mode)

The APU-FDX-2 module ports can be configured in chronological receive mode to sequentially receive frames and store them in a circular buffer. The payload data can be discarded to optimise the use of the buffer for frame capture and analysis. Powerful filtering, triggering, complex triggering and capture modes allows users to select only the frames, data and errors of interest. Monitor mode also provides activity monitoring and statistics for each VL recorded by the APU-FDX-2 module. The interface modules report the number of frames received and the number of errors detected globally and in VL orientated format.

- *VL orientated Receive and Filtering*
- *Second Level Filtering on Generic Frame Parameters*
- *Chronological Monitor with Time Stamping to 1µs*
- *Massive onboard Monitor Buffer*
- *Inter Frame Gap Time Measurements with 40ns Resolution*
- *Comprehensive Triggering/ Filtering/ Capturing*
- *Programmable Data Capture Modes - Trace after Trigger & Recording*
- *Physical Error Detection - CRC, Gap, Size and Alignment*
- *AFDX/ ARINC664 Specific Error Detection*

## Application Support Processor

The 600 MHz Application Support Processor (ASP) provides unique on-module processing functions typically provided by host PC processing systems.

- *IP and UDP layer of the AFDX/ ARINC664 protocol*
- *Driver Software Execution onboard*
- *Dynamic Data Generation*
- *Loop/ Pollution between Rx and Tx Port*
- *Automatic Test Sequence Generation*
- *Program using Real Time Operating Systems*

## IRIG-B Time Code Decoder

APU-FDX-2 modules include an onboard IRIG-B time encoder/ decoder with sinusoidal output and 'free wheeling' mode for time tag synchronisation. This allows synchronisation of multiple APU-FDX-2 modules to any IRIG-B time input source or to the onboard time code generator of one APU-FDX-2 module as the reference for the correlation of data across multiple AFDX/ ARINC664 ports.

## Driver Software Support

A full function Application Programming Interface (API) is provided compatible with Windows and Linux. Drivers for other operating systems especially used in embedded applications are available upon request. Please contact the factory for further details on driver availability for a particular operating system and host platform. Host applications for the APU-FDX-2 can be written in C and C++.

# APU-FDX-2

*USB Module for AFDX/ ARINC664 Test & Simulation*

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## *Technical Data*

**USB2.0 Interface:** 480Mbit USB2.0 Standard Interface (Revision 2.0)

**Processors:** Two 32-bit, 600MHz RISC Processors

**Memory:** 64MB Global RAM, 64MB ASP RAM

**Encoder/Decoder**: Two AFDX/ ARINC664 specific Ethernet MAC's
- Inter Frame Gap generation and measurement with 40ns resolution

**Time Tagging:** 46-bit absolute IRIG-B time with 1$\mu$s resolution

**Physical Bus Interface:**
Two full duplex AFDX/ ARINC664 ports configurable to one dual-redundant AFDX/ ARINC664 port

**Connectors:**
- 2 x 8-way RJ45 connectors, one per AFDX/ ARINC664 port
- 1x 15-way High Density D-Sub connector (female) for Time Code and Trigger I/O

**USB-Connector:** USB-Connector (B-Type)

**Dimensions:** 153mm x 85mm x 19mm

**Power Consumption:** typical 4,5W

**Operating Temp. Range:**
Standard: 0°C... +55°C ambient. Extended: -15°C...+60°C ambient

**Storage Temp. Range:** -40°C ... +85°C ambient

**Humidity:** 0 to 95% non-condensing

## *Ordering Information*

**APU-FDX-2**
Two Port, USB2.0 to AFDX/ ARINC664 Interface:
Traffic Simulator, Receiver and Chronological Monitor
64MB Global RAM, 64MB ASP RAM
Including USB Cable (1.2m, occupying two USB Ports)
*Includes Driver Software for WindowsXP/Vista/7, LabVIEW VI's, Linux*

**APU-FDX-2B**
Two Port, USB2.0 to AFDX/ ARINC664 Interface:
Traffic Simulator, Receiver and Chronological Monitor
64MB Global RAM, 64MB ASP RAM
Including Boeing B787 Specific Extensions
Including USB Cable (1.2m, occupying two USB Ports)
*Includes Driver Software for WindowsXP/Vista/7, LabVIEW VI's, Linux*