Model 56720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - AMC

General Information

Model 56720 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/A and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56720 includes a front panel general-purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56760 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56720 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

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Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clockSYNC bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-7 FPGA for custom I/O
**A/D Acquisition IP Modules**

The 56720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 56720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/A's waveform stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ **GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ➤
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Memory Resources
The 56720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

AMC Interface
The Model 56720 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface
The Model 56720 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

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Ordering Information

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Options:
-073  | XC7VX330T-2 FPGA |
-076  | XC7VX690T-2 FPGA |
-104  | LVDS FPGA I/O through front panel connector |

D/A Converters
- **Type**: Texas Instruments DAC5688
- **Input Data Rate**: 250 MHz max.
- **Output IF**: DC to 400 MHz max.
- **Output Signal**: 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate**: 800 MHz max. with interpolation
- **Resolution**: 16 bits

Front Panel Analog Signal Outputs
- **Output Type**: Transformer-coupled, front panel female SSMC connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Output**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard**: Xilinx Virtex-7 XC7VX330T-2
- **Optional**: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104**: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Type**: DDR3 SDRAM
- **Size**: Four banks, 1 GB each
- **Speed**: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus**: Gen. 1, 2 or 3: x4 or x8; Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

AMC Interface
- **Type**: AMC.1
- **Module Management**: IPMI Version 2.0

Environmental
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: Single-width, full-height AMC module, 2.89 in. x 7.11 in.
70 MHz, f_s = 200 MHz, Internal Clock

30 MHz, f_s = 200 MHz

70 MHz, f_s = 200 MHz, Internal Clock

69 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk

70 MHz, f_s = 200 MHz, Ch1 shown

Input Frequency Response

f_s = 200 MHz, Internal Clock

70 MHz, f_s = 200 MHz, Internal Clock

140 MHz, f_s = 400 MHz, External Clock

D/A Performance

Spurious Free Dynamic Range

Spurious Free Dynamic Range